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Ver: 3.1

ATX (243.84x304.8) mm

Intel Skylake Platform (Z170-XPOWER)

CPU:Socket H4

2015 Skylake LGA1151

Main Memory:

Dual Channel DDR4 * 4 (Max 32G)

Power Solution:

CPU : IR35201 +IIR3599 (10+4)
VCCSA : POWERVATION 3205Q (2PH)
VCCIO : MPS NB685
VCCST : GS7116
VCCPLL : GS7116
DDR : POWERVATION 3205Q (2PH)
PCH : UPI UP1540

ACPI:

3VDSW : GS7166
5VDUAL : UP7501
3VSB : MP2147

Onboard Chip:

Clock Gen : IDT6V41516
Clock Gen : IDT-VC3
SATA Express : ASM1061
USB3.1 Host : ASM1142A
LAN : Intel i219
HD Codec:ALC1150 + AMP
SIO:Nuvoton 6793D
USB Charger : SLG55583A * 2
USB Redrive : ASM1464 * 4
HDMI:PTN3360D * 2
HotKey:F75501
Flash BIOS:F75504
GPIO : NCT5605 * 2

Expansion Slots:

PCI Express (X16) Slot * 3 (16/8+8/8+4+4)
PCI Express (X1) Slot * 3
PCI Express (X4) Slot * 1
M.2 Slot (Socket 3) * 2 (Share SATA)

PCH:Z170 FCBGA837

Z170
SPI ROM: 128 MB + 128 MB

Rear I/O Connectors


PS2 + Dual USB2
Clear COMS
Reflash BIOS USB2
Dual USB3 + HDMI
RJ45 + Dual USB3
DP+HDMI
Dual USB3.1
Audio Jack 5 Port +SPDIF

Internal Connectors

Dual SATA Express * 1
Dual SATA * 2
FUSB2 Header * 2
FUSB3 Header * 1
Front Audio Header * 1
Front Panel Header * 2
OC Dash Board * 1
SPI Header * 1
TPM Header * 1
CPU Fan * 2
System Fan * 3
Vcheck points

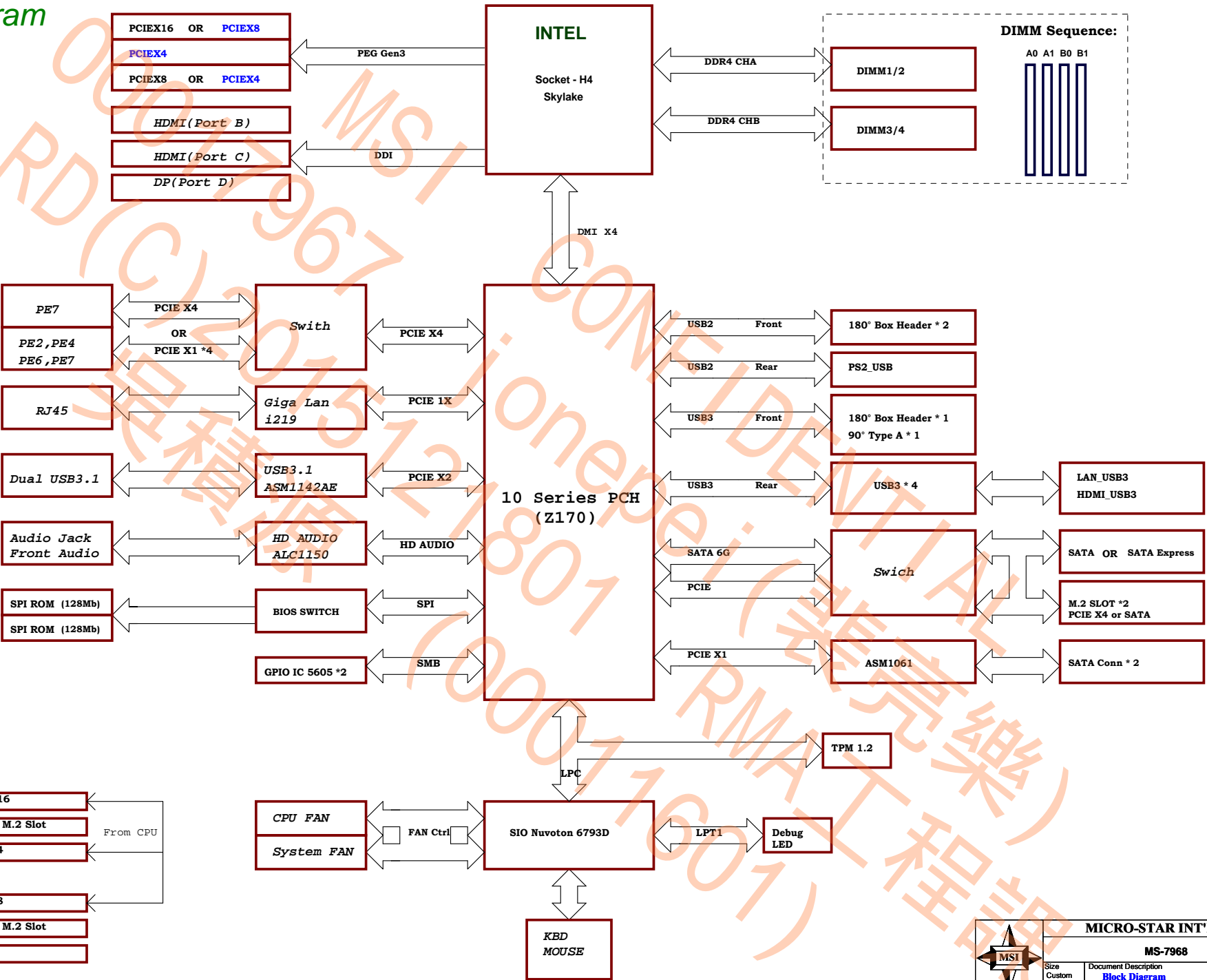
Bottom

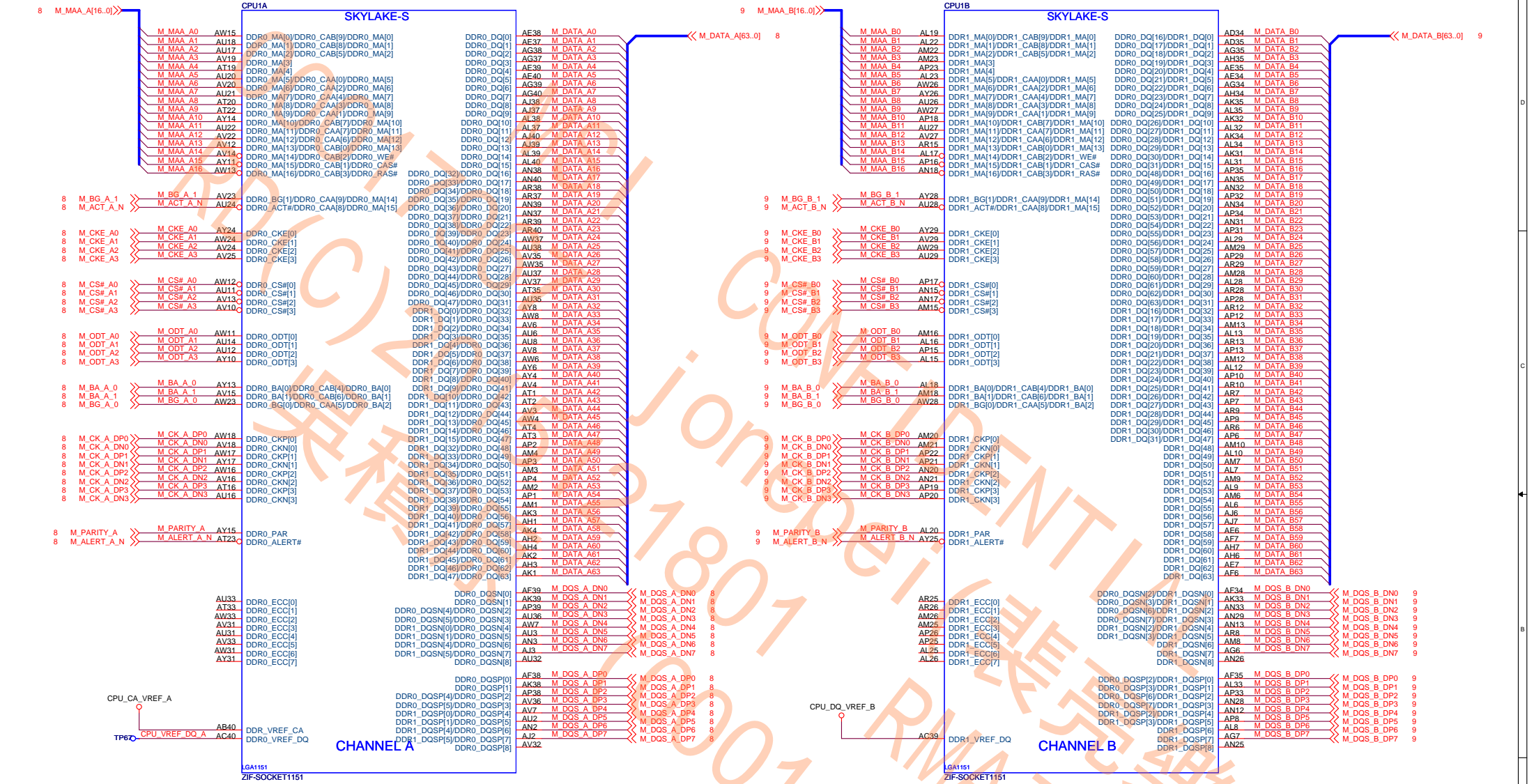
Power
Reset
Gaming Boost
Switch
Dual BIOS
LED
Debug LED
HOTKEY

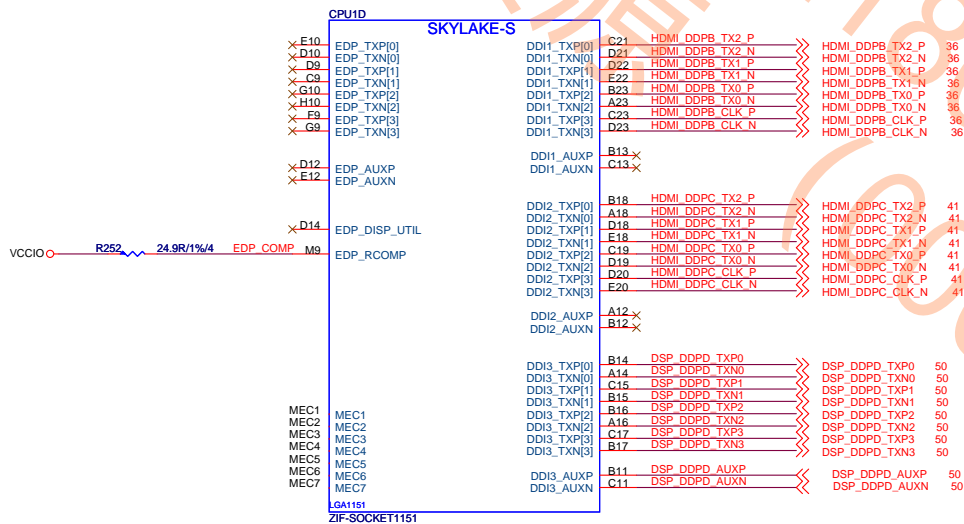
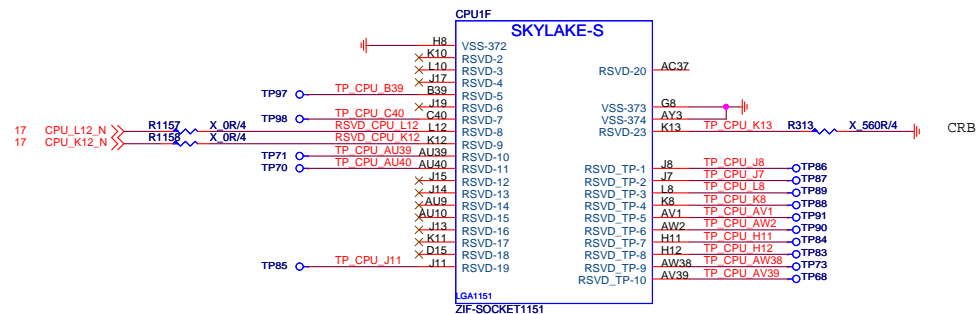
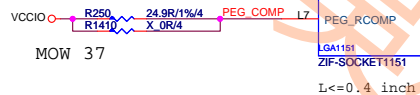
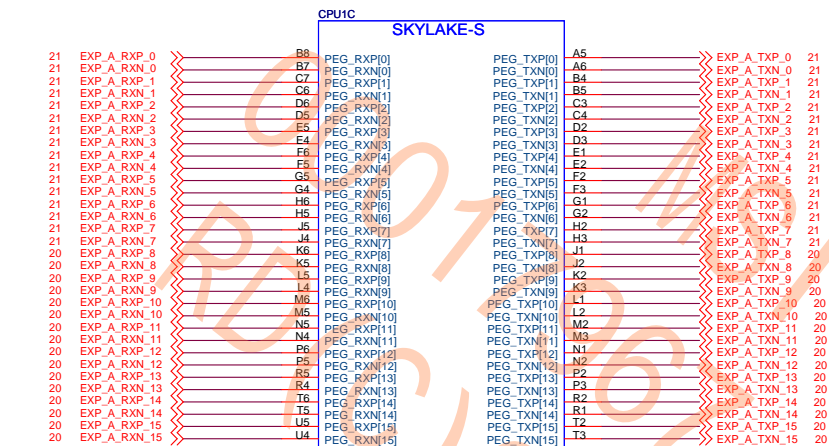


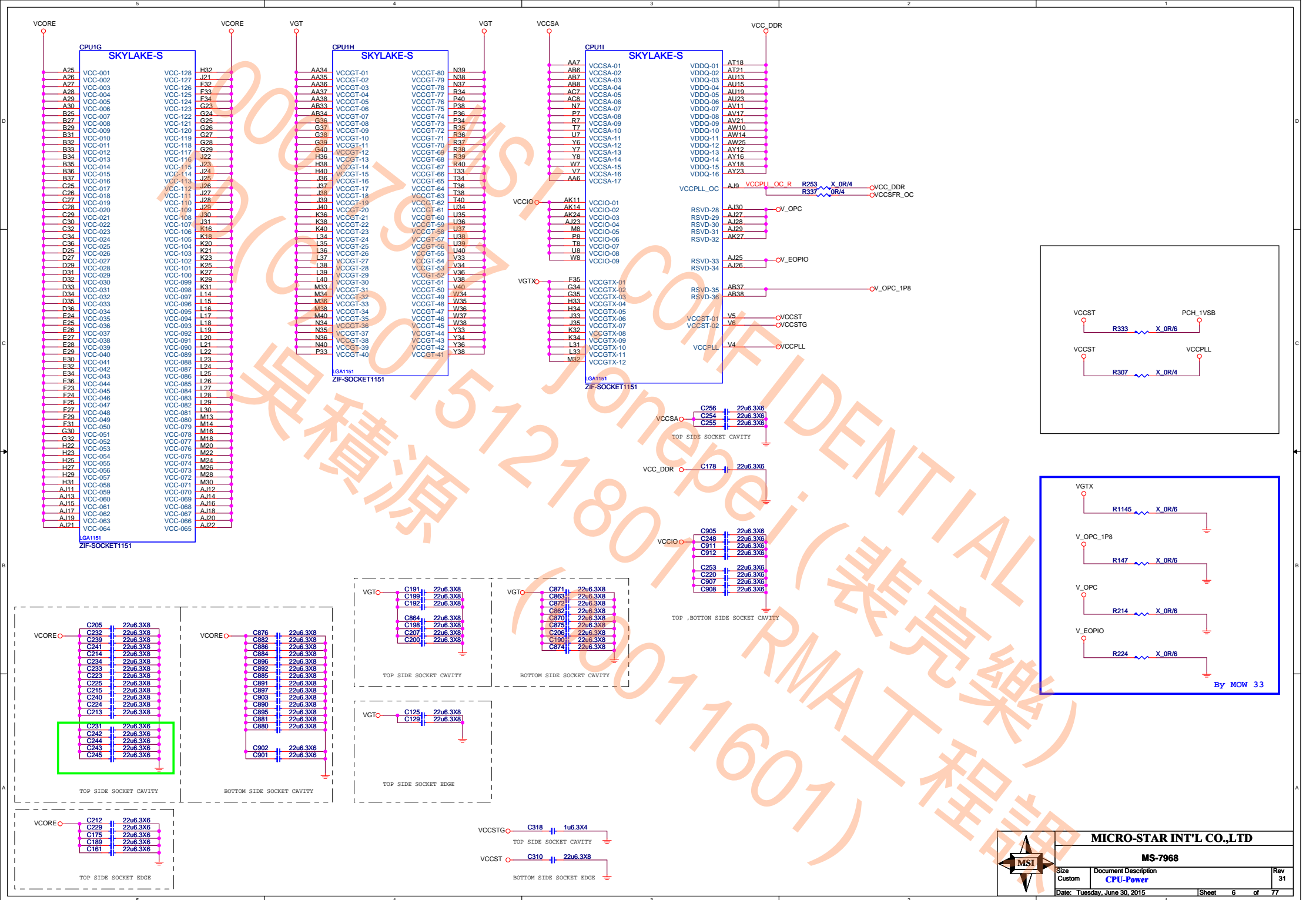
MICRO-STAR INT'L CO.,LTD		
MS-7968		
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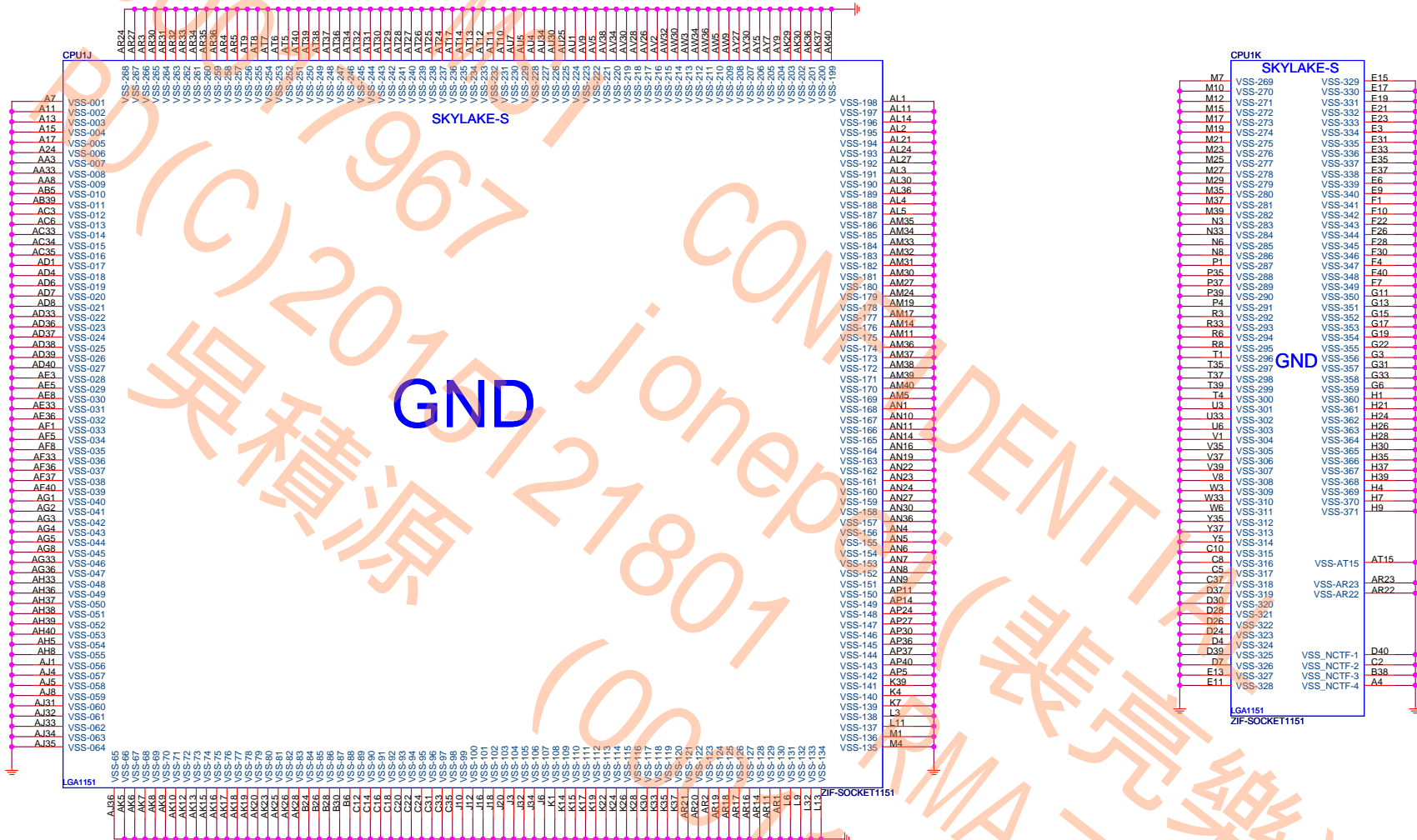
MS-7968 3.0
Block Diagram

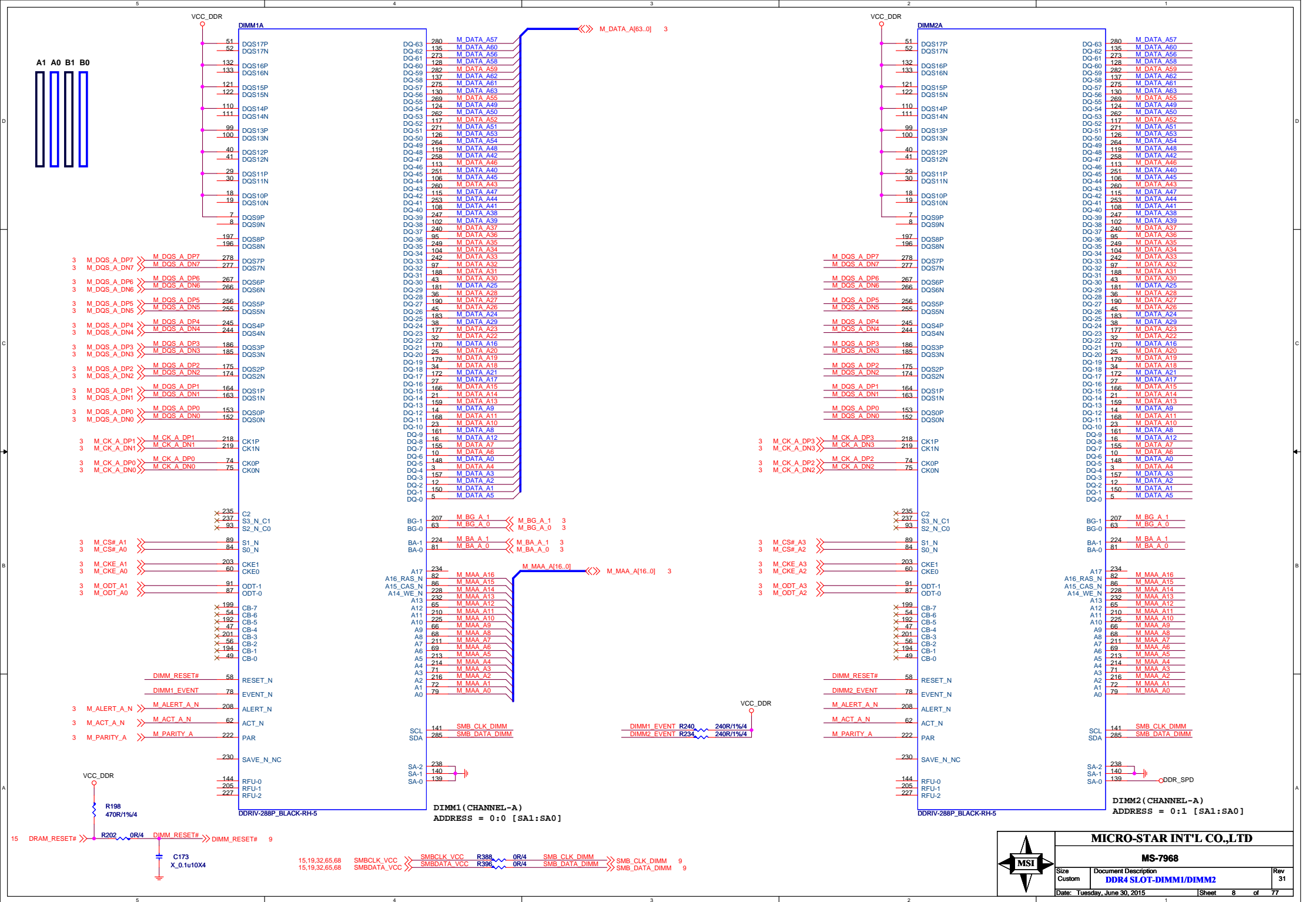












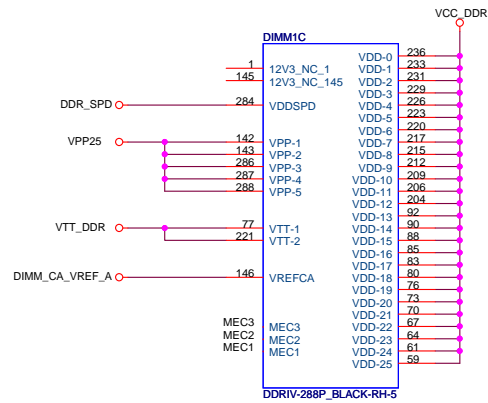
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4

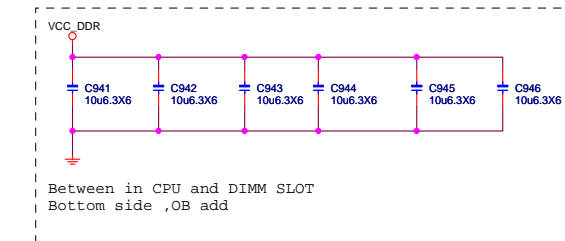
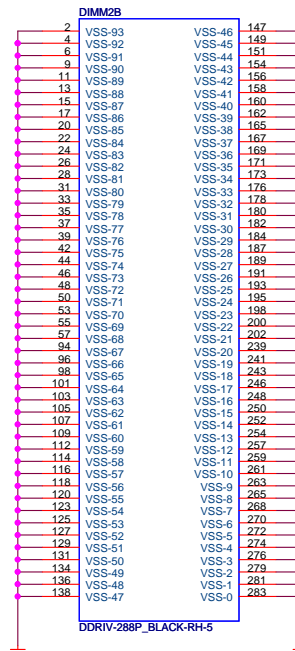
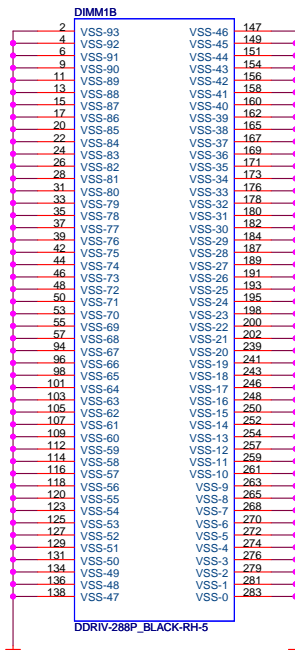
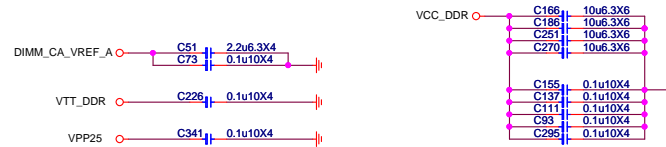
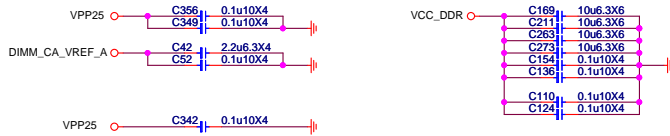
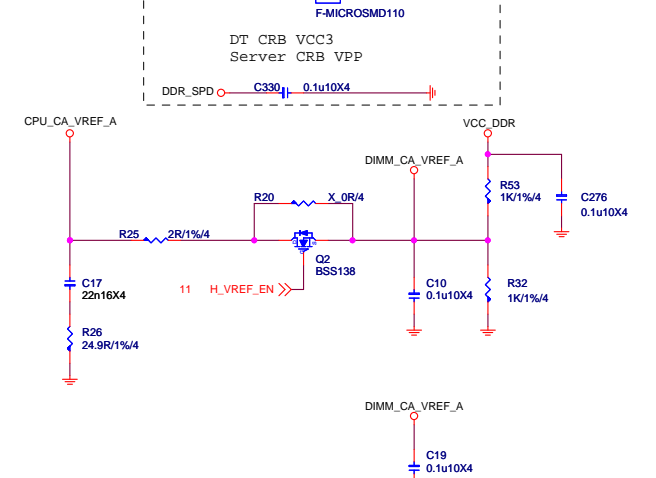
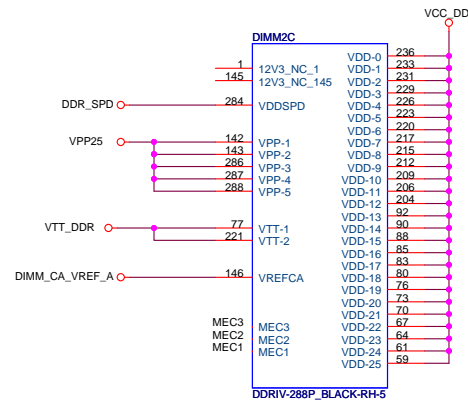
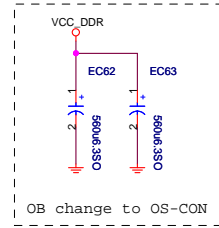
3

2

1



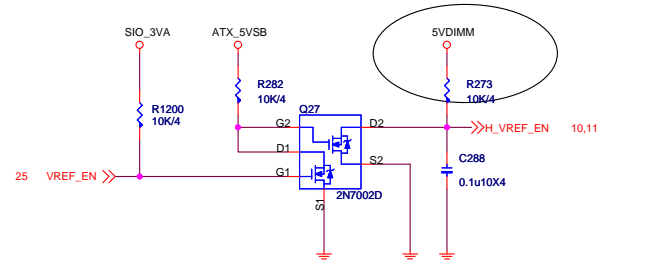
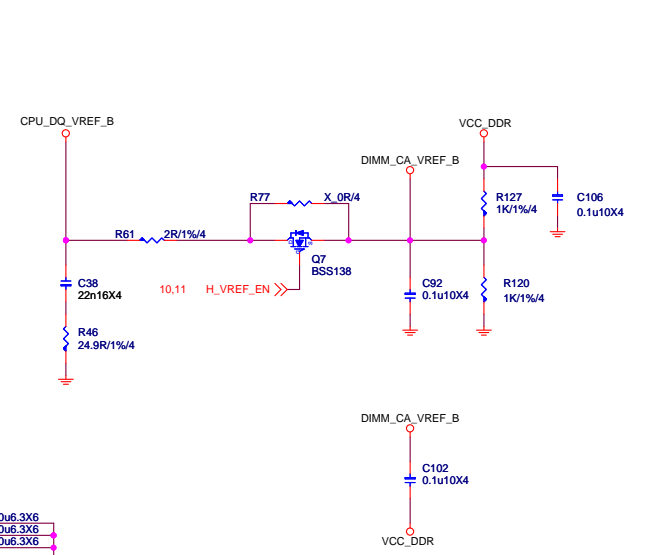
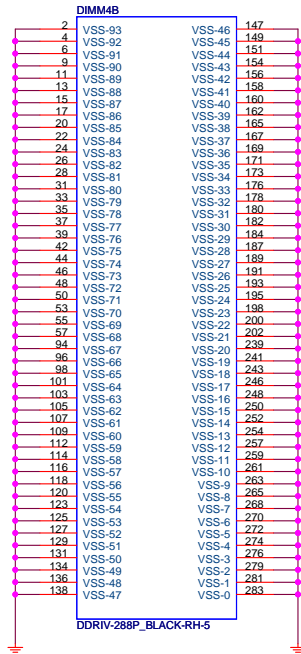
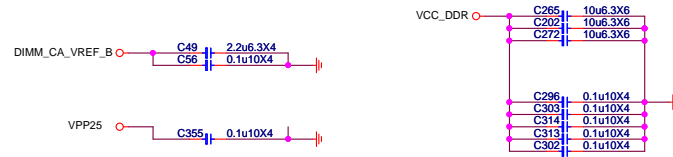
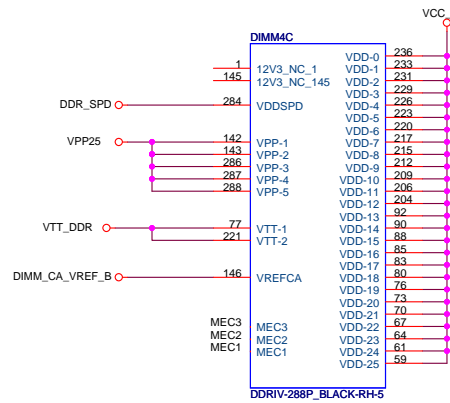
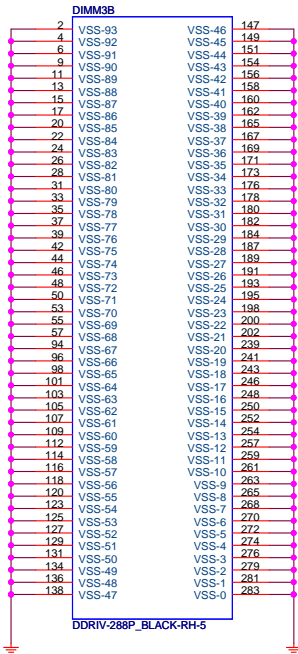
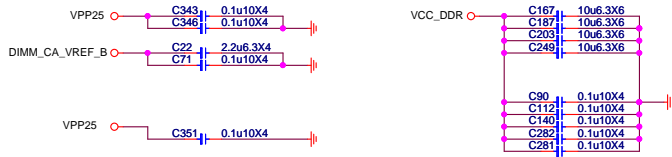
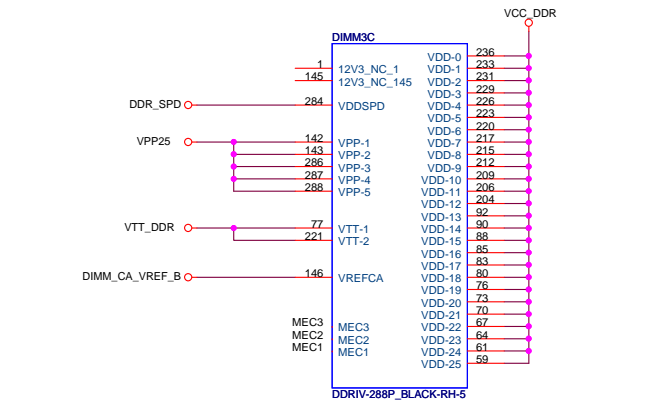
DIMM SLOT PN BY SPEC



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GPP_I[3:0] with SMI/NMI

PCH1D

SPT-H_PCH

Port B

Port C

Port D

AUDIO

eDP

4 OF 10

SPT-H

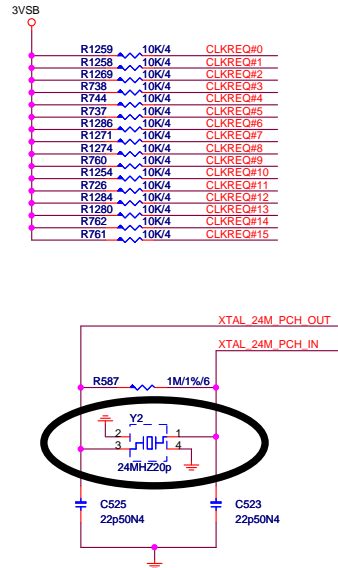
PCH1C

SPT-H_PCH

Clock

3 OF 10

SPT-H

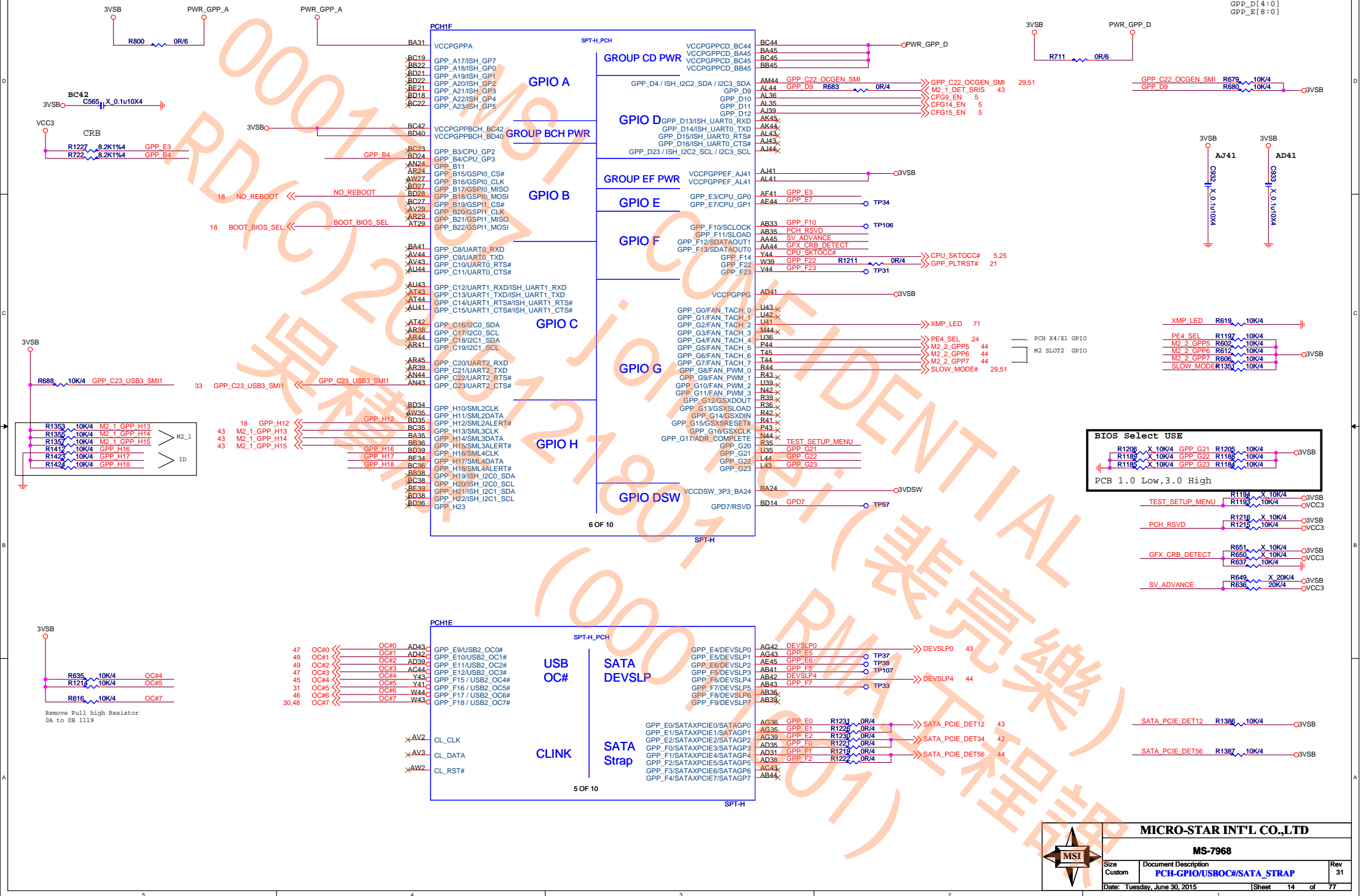


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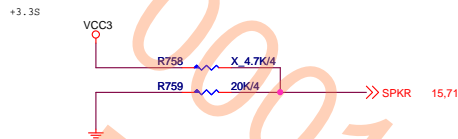
GPP_B[23,20,14]
GPP_C[23:22]
GPP_D[4:0]
GPP_E[8:0]



GND

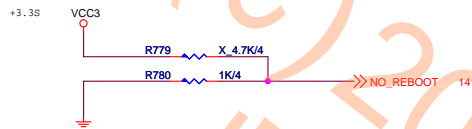
10 OF 10

TOP Swap



Internal pull-down is disabled after PLTRST#

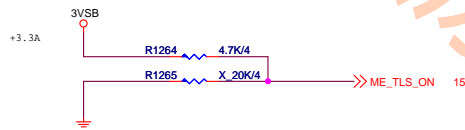
No Reboot



0 : DISABLE (Default)
1 : ENABLE

Internal pull-down is disabled after PLTRST#

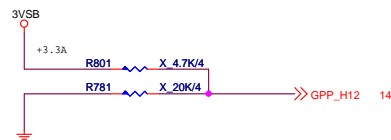
AMT and SBA with confidentiality



0 : DISABLE
1 : ENABLE (Default)

Internal pull-down is disabled after RSMRST

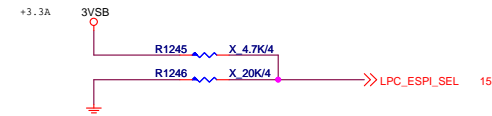
ESPI FLASH SHARING MODE



0 : MASTER ATTACHED FLASH SHARING
1 : SLAVE ATTACHED FLASH SHARING

Internal pull-down is disabled after RSMRST

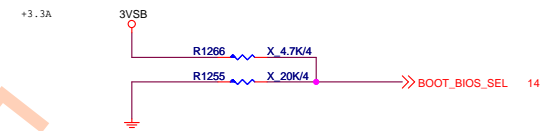
LPC eSPI Mode



0 : LPC
1 : eSPI

Internal pull-down is disabled after RSMRST

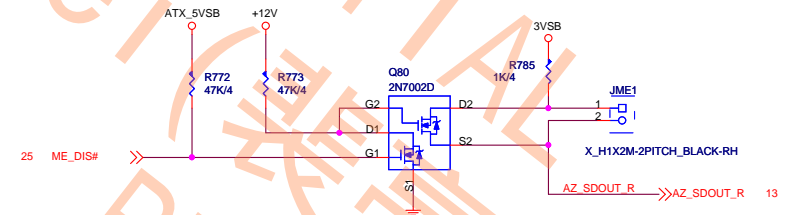
Boot BIOS



0 : SPI
1 : LPC

Internal pull-down is disabled after PLTRST

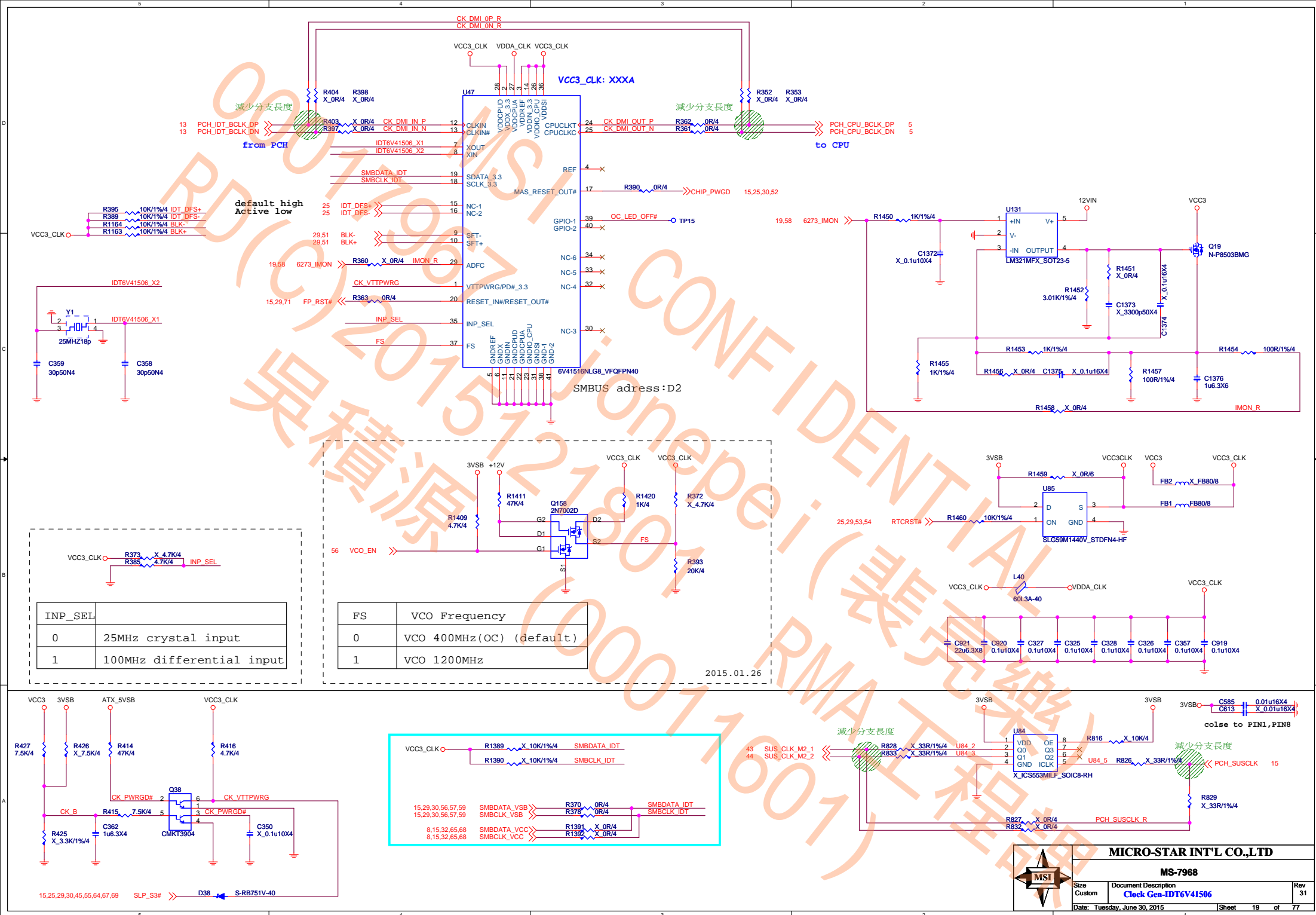
HDA_SDO

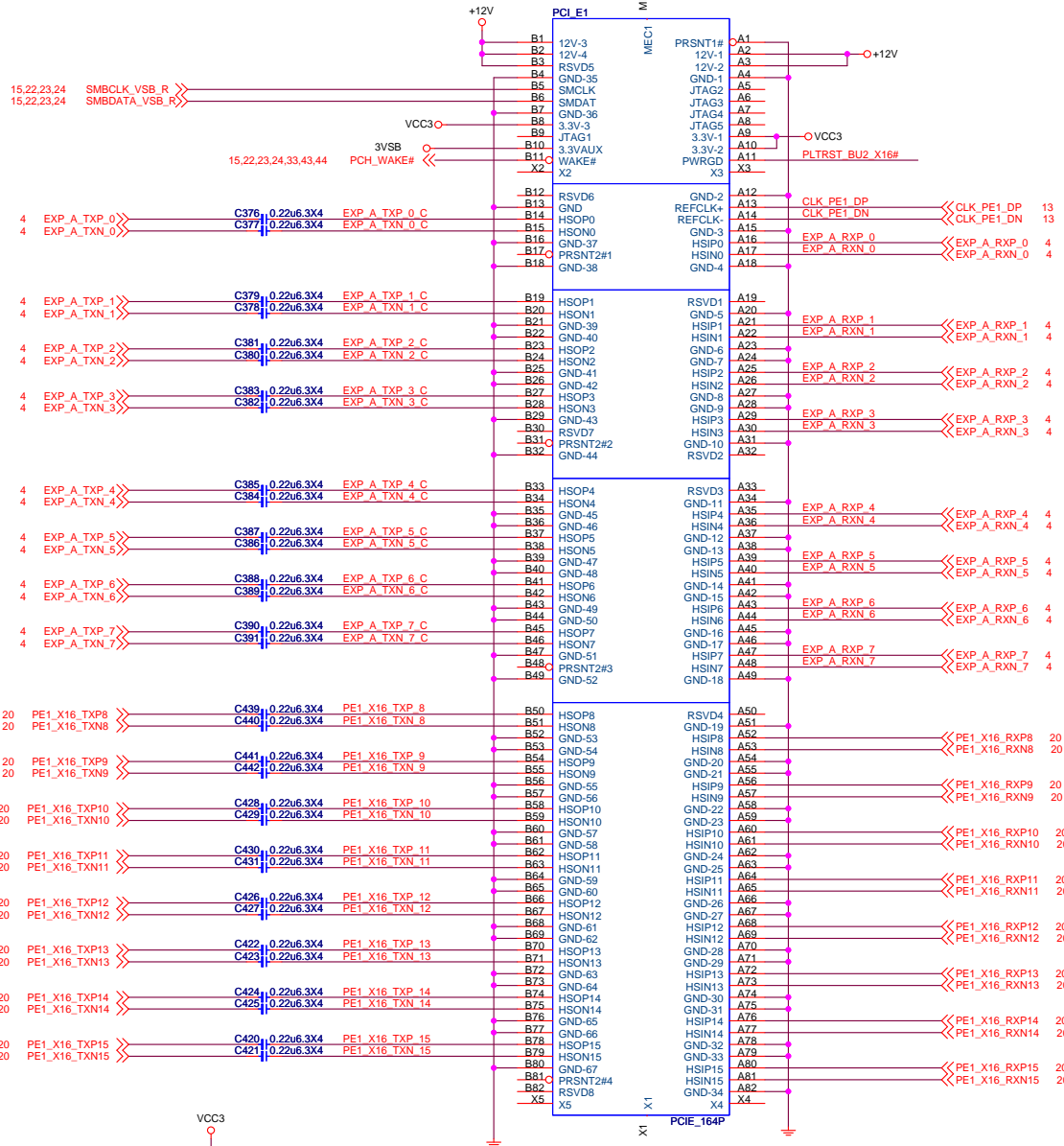
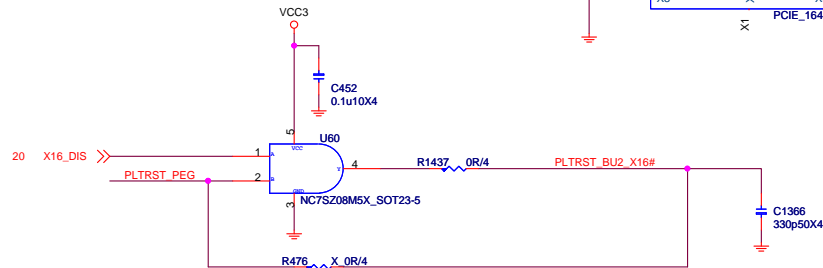
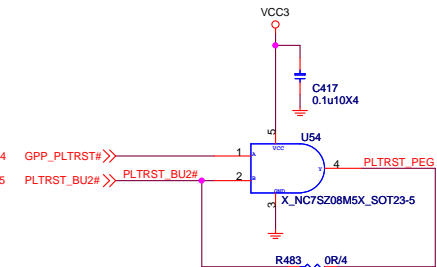
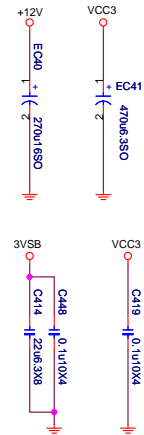
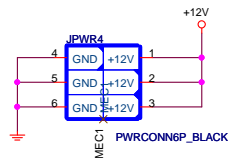


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(Share with PCI E x16 Slots)



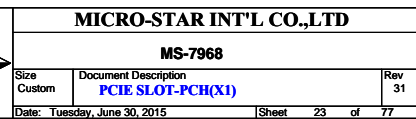
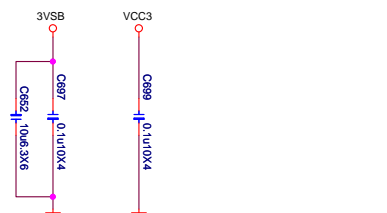
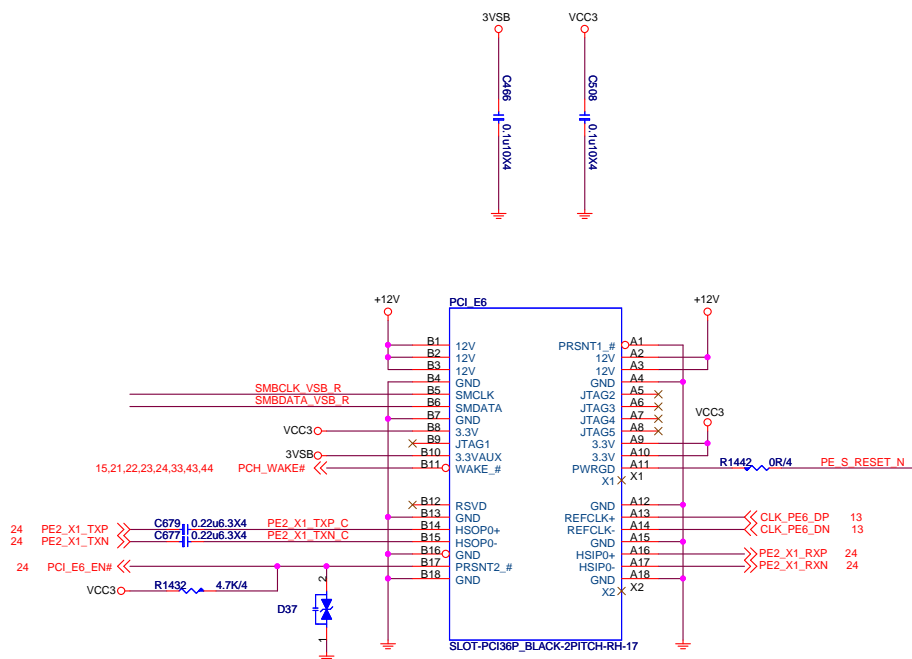
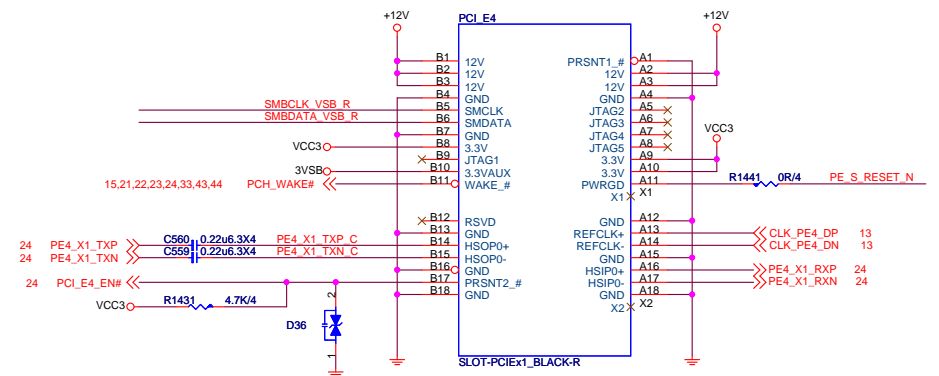
PCI_Express X4 slot(by CPU)



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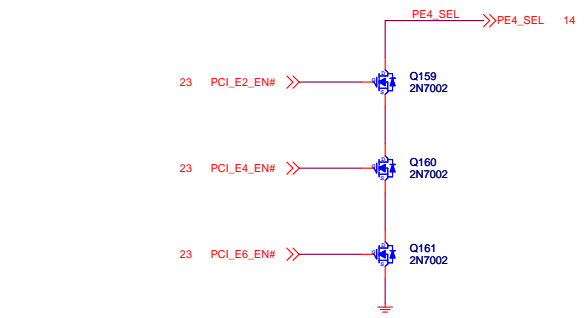
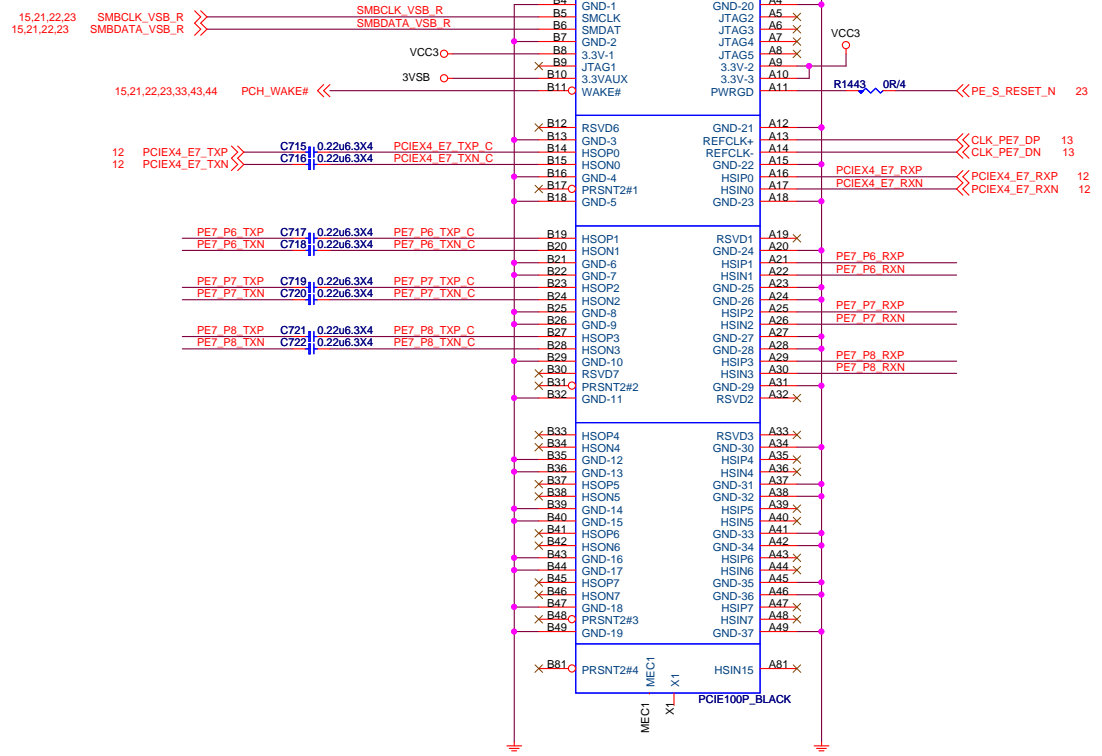
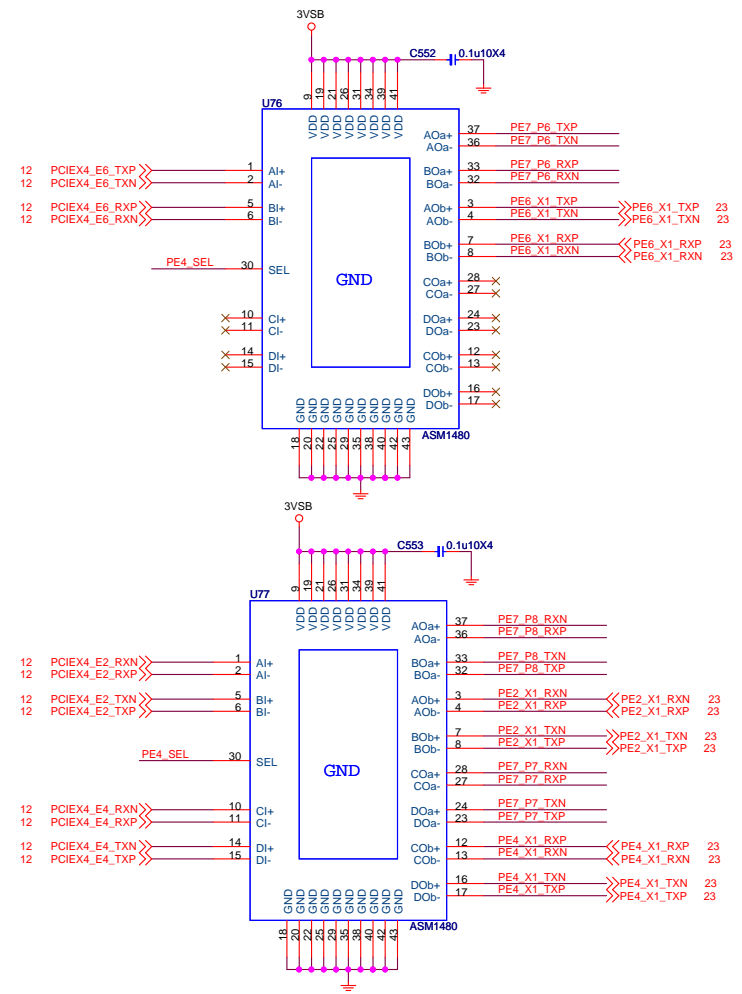
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Size Custom	Document Description PCIE SLOT-CPU(X8)(X4)	Rev 31
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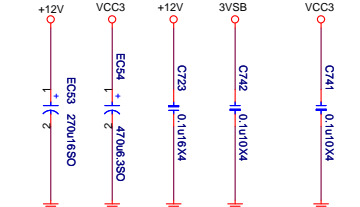
PCI_Express X4 Slot

12V - 2.1A
VCC3 - 3A
3VSBV - 375mA



X1 Mode PE2,PE4,PE6,PE7 Working (Default)
X4 Mode PE7 Working

	HW		SW	
	X1	X4	X1	X4
PE4_SEL	High (GPI)	Low (GPI)	High (GPO)	Low (GPO)

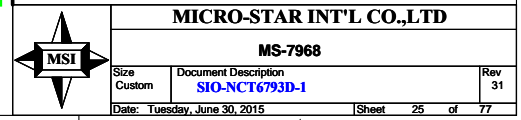
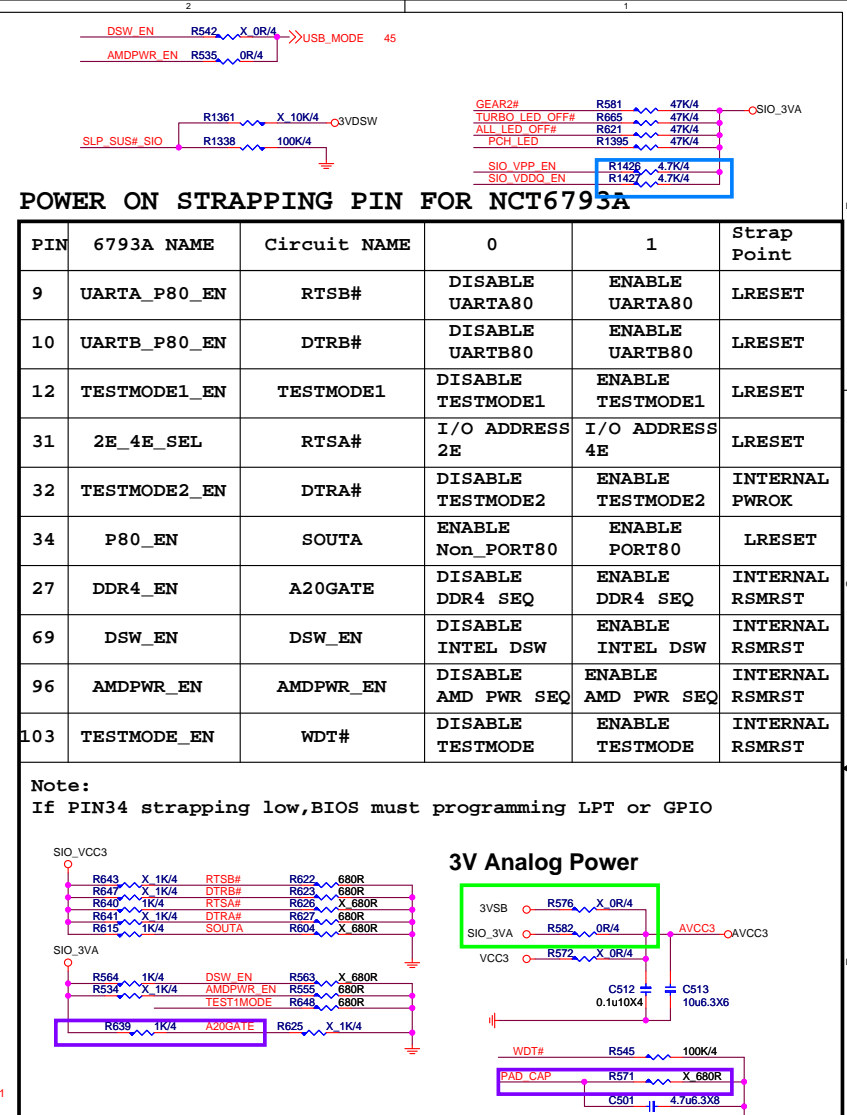


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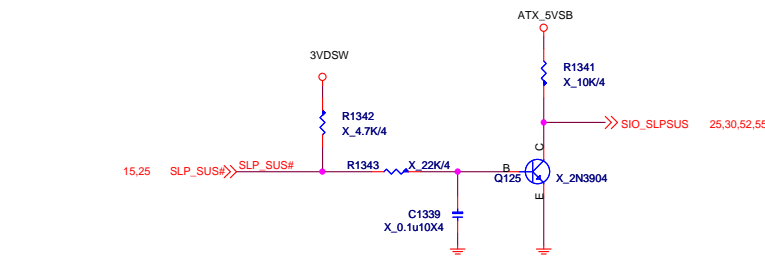
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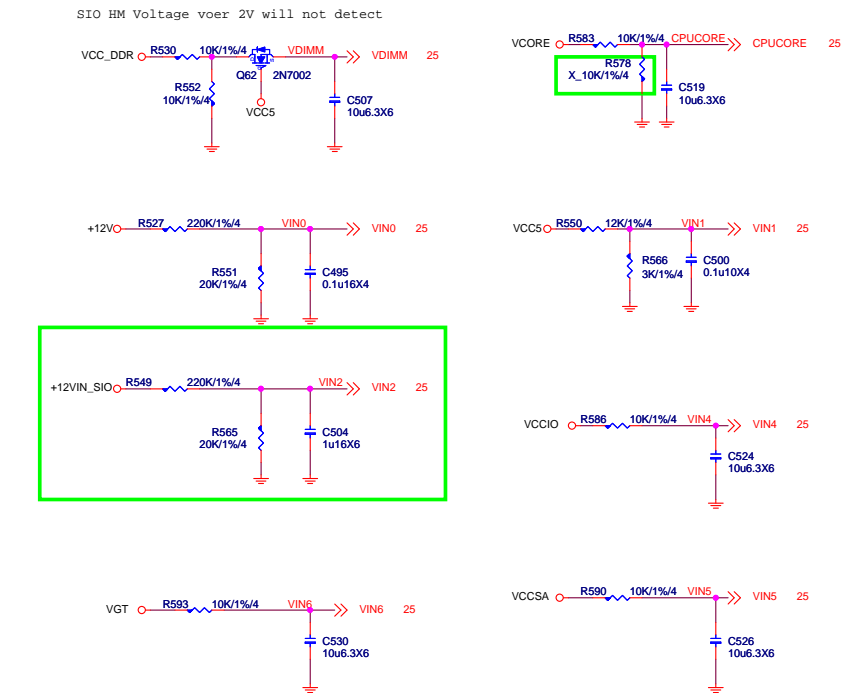
COM Port for BIOS Debug



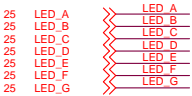
SLP_SUS Co-lay circuit



HW Monitor - Voltage

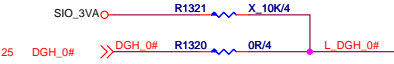
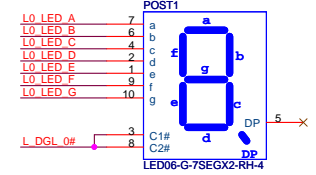
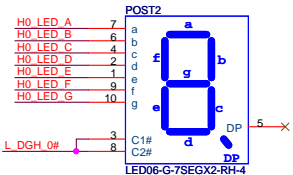


DEBUG LED



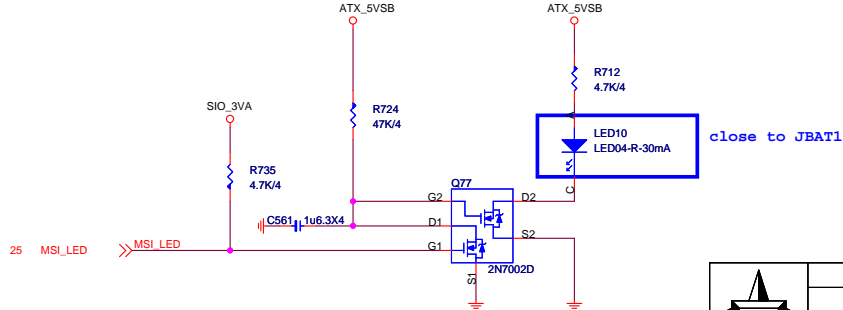
Placement一定要對
(DGH1=Post4/DGL1=Post3/DGH0=Post2/DGL0=Post1)

Debug LED OFF BIOS control



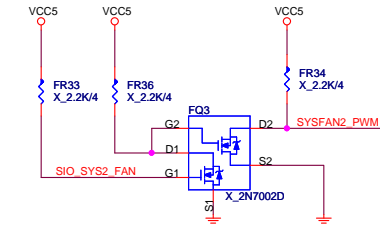
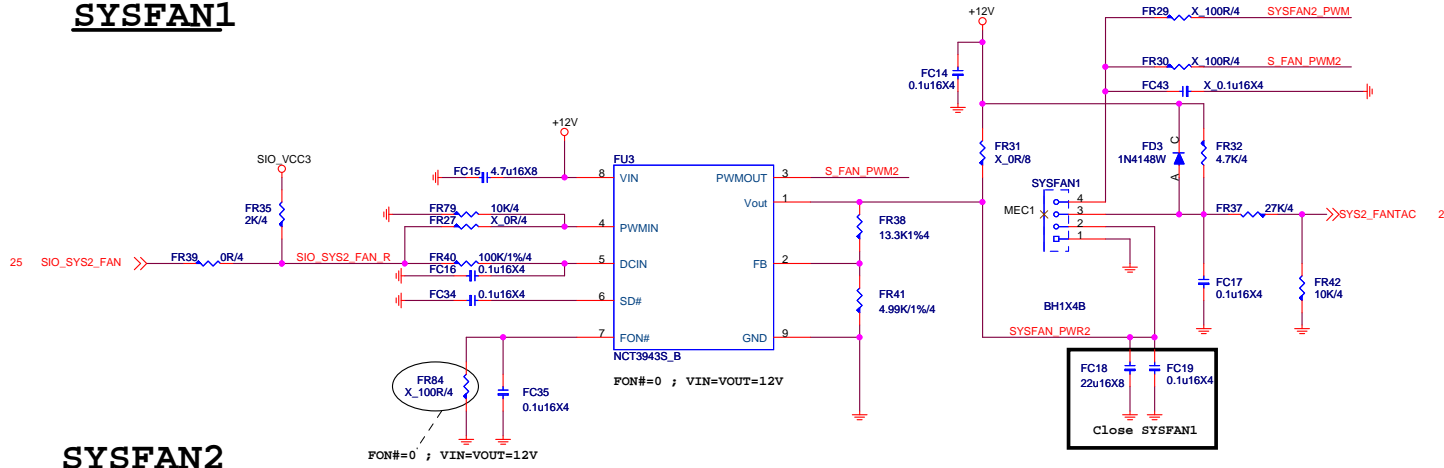
Ver 3.0
Remove Post3,Post4

MSI_LED

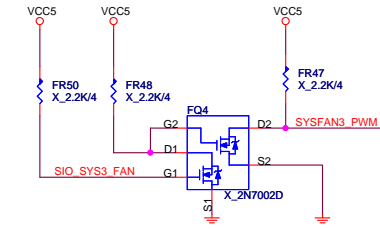
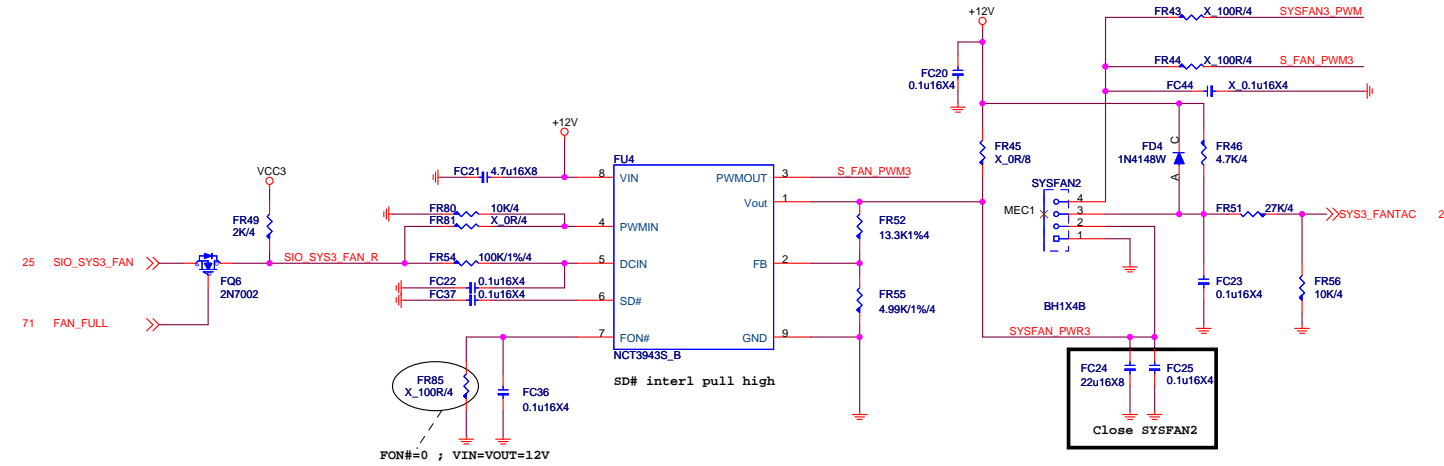


Type H : 4 PIN SYS FAN FROM NCT3943S

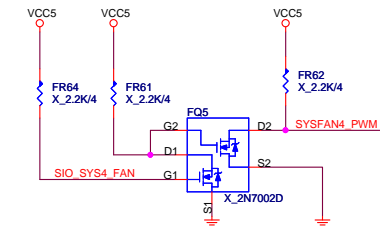
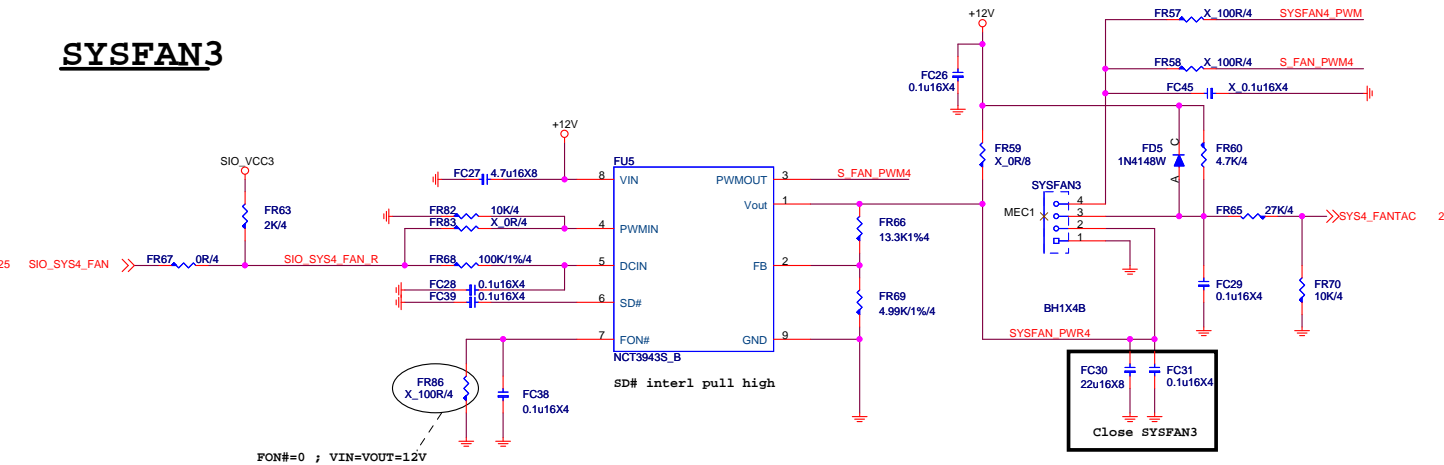
SYSFAN1

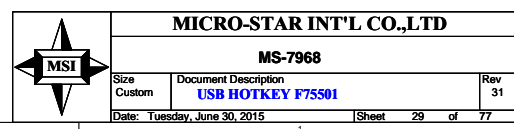


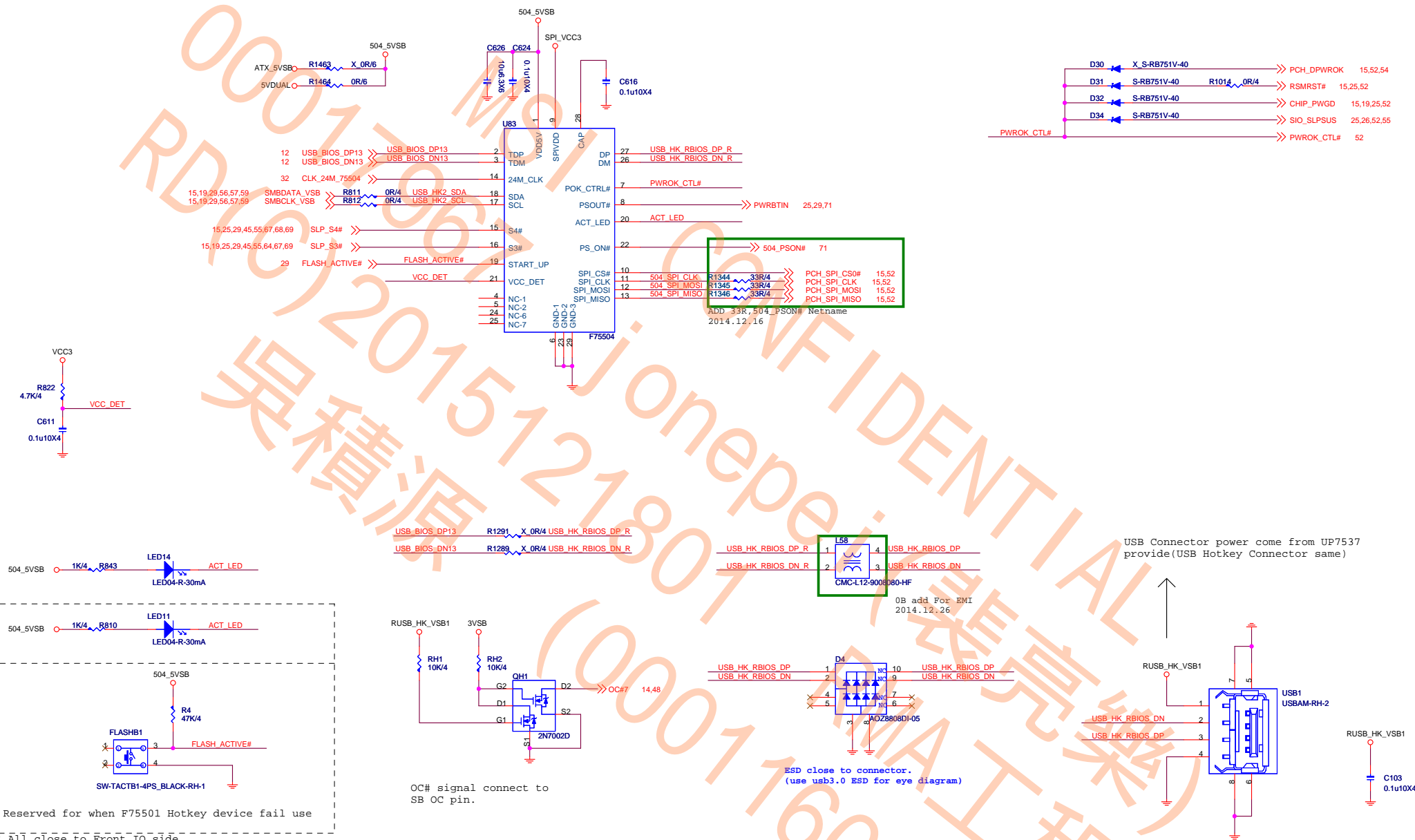
SYSFAN2



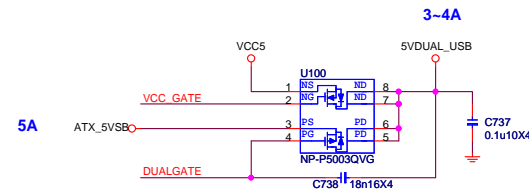
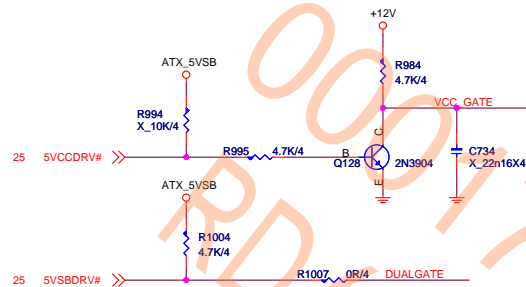
SYSFAN3



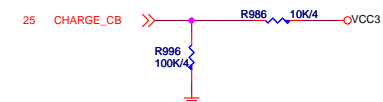




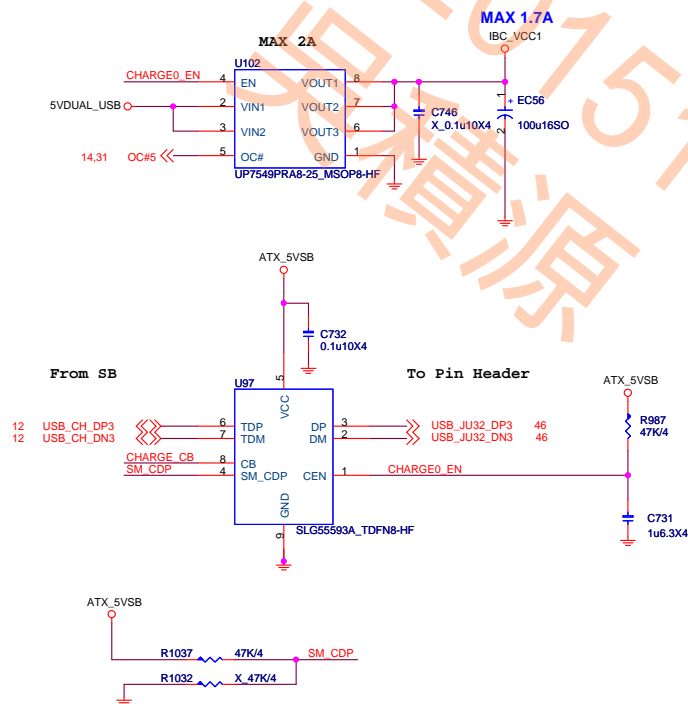
5VDUAL_USB



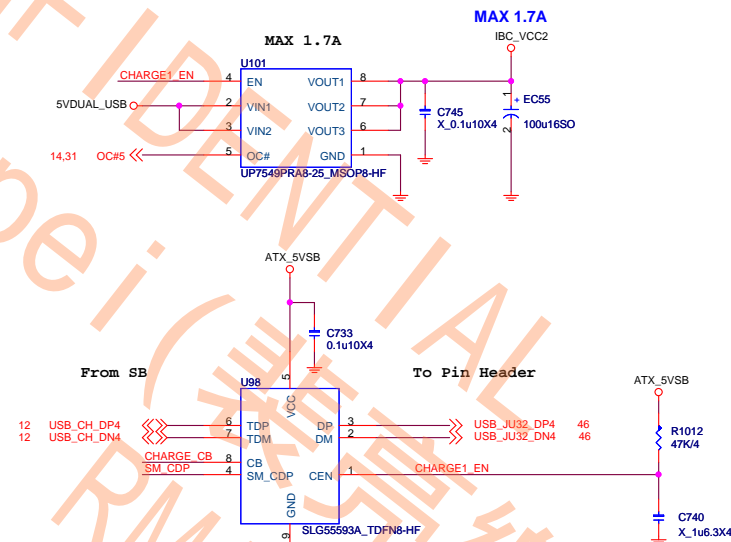
Pin power : I_3VSB
Register power : I_3VSB
Register reset : I_3VSB



USB POWER PORT 0 For USB Charging



USB POWER PORT 1 For USB Charging

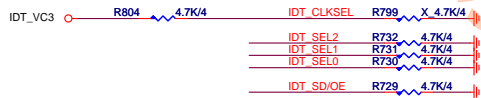
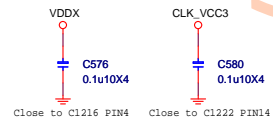
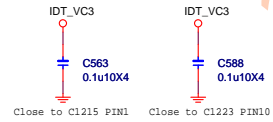
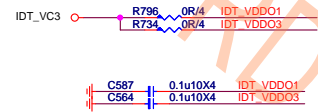


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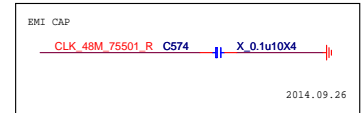
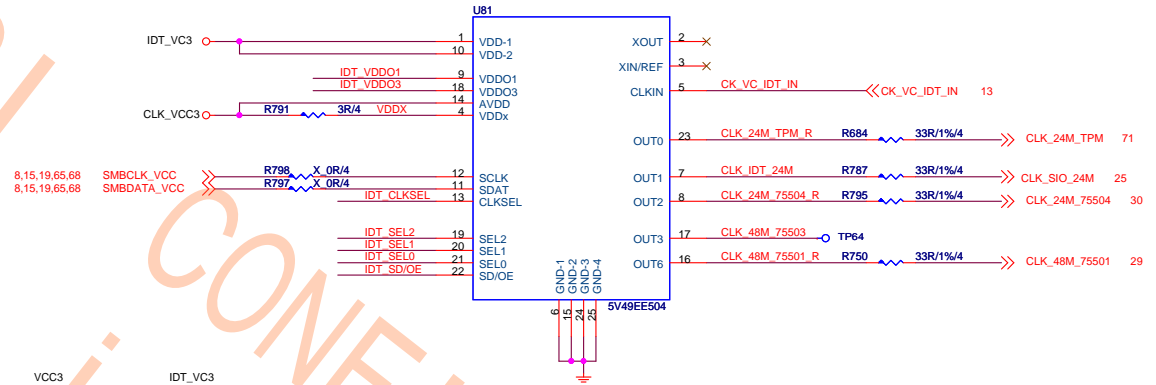
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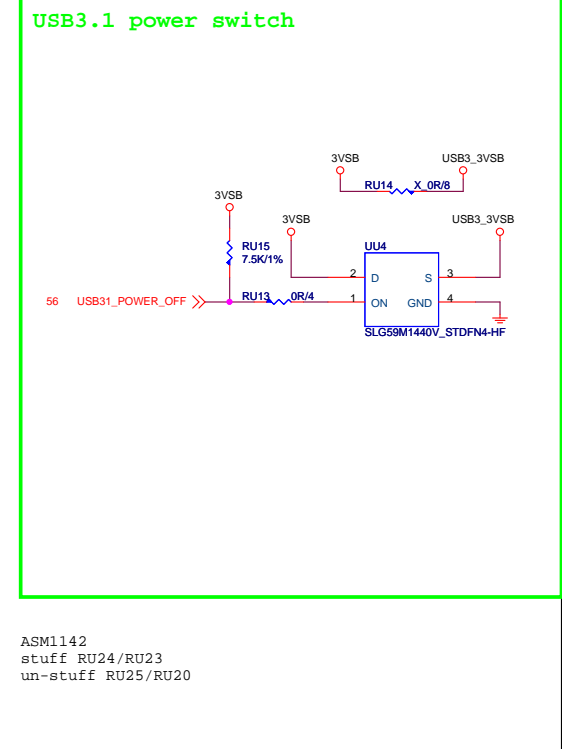
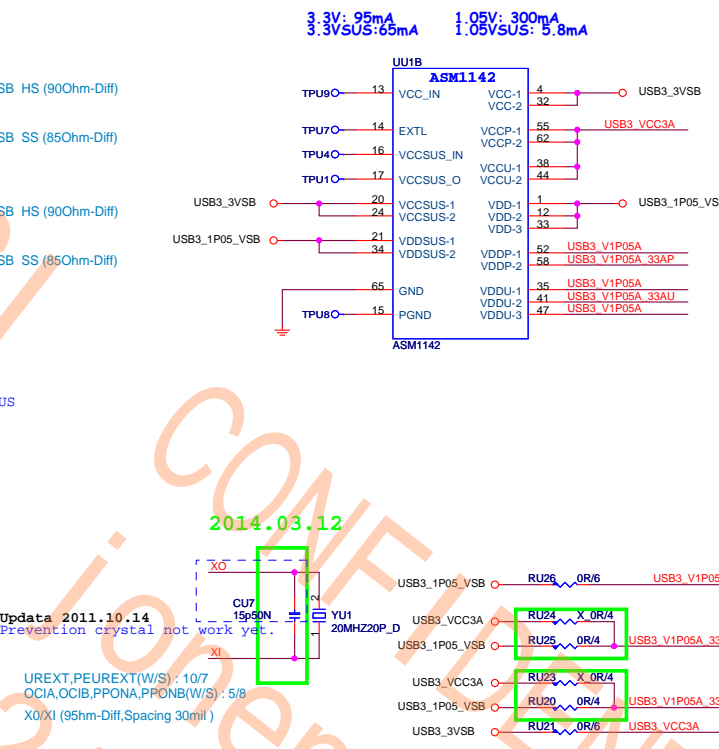
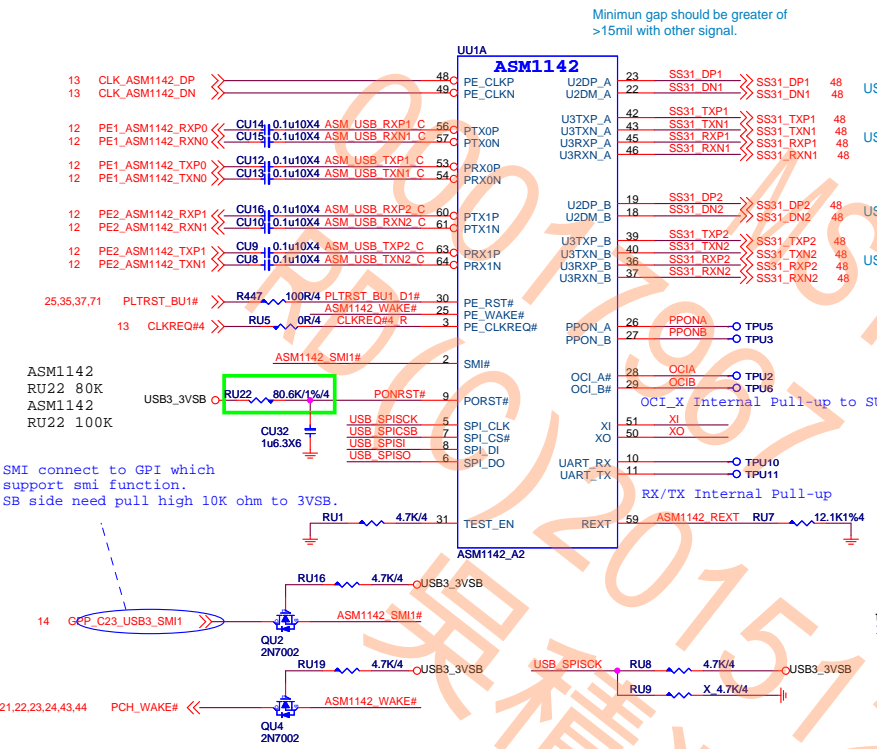
CLK GEN



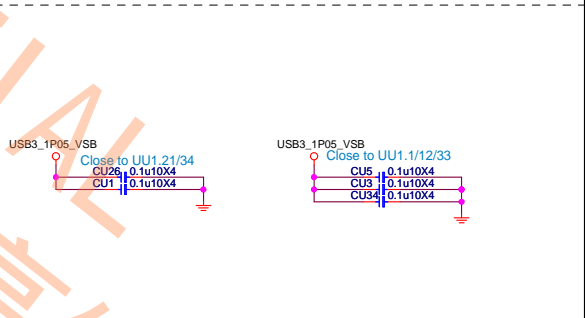
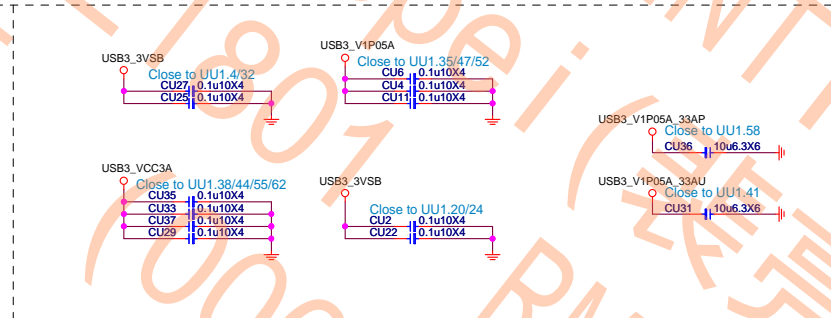
Clock Gen PN not final



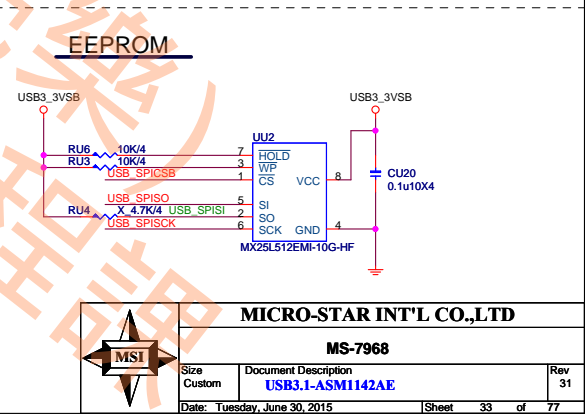
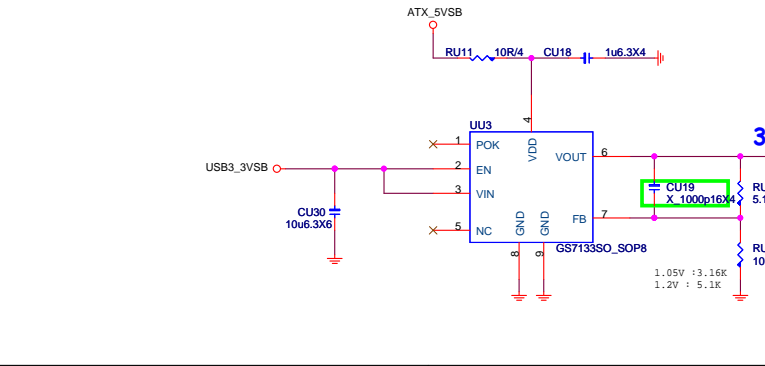
Remove X'tal 0B



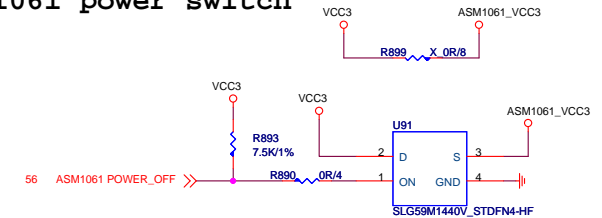
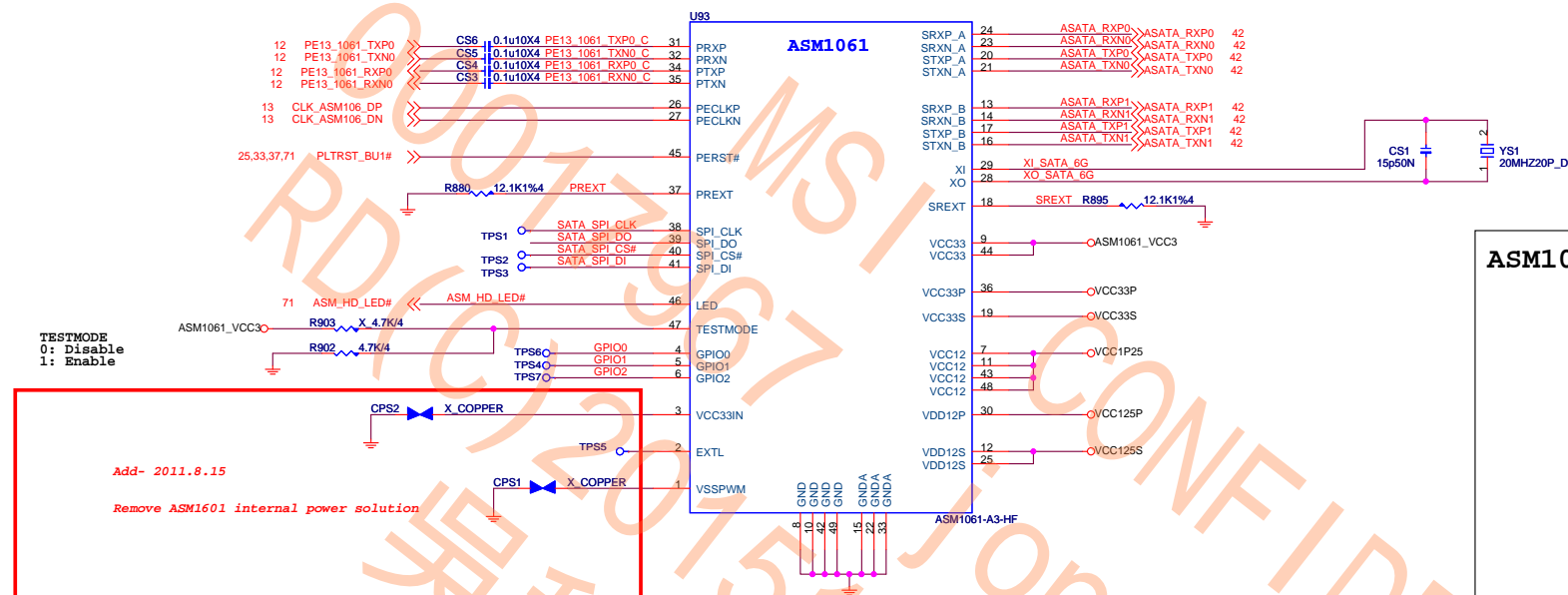
ASM1042 3VSB Circuit



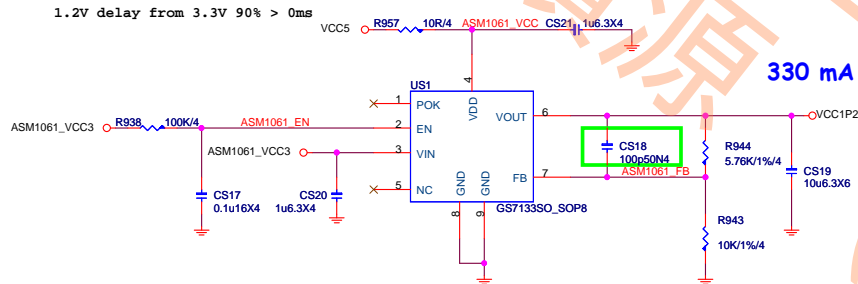
ASM1042 1.2VSB Power



ASM1061 SATA6G

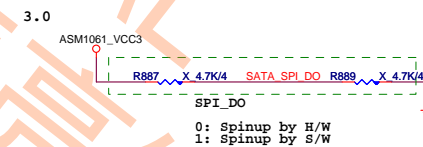
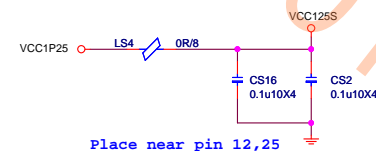
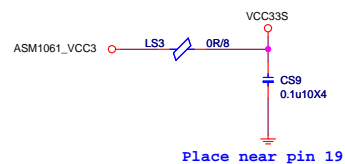
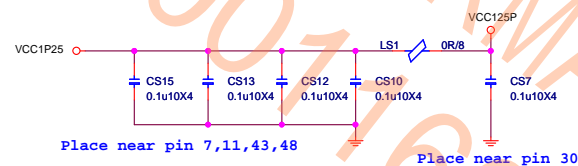
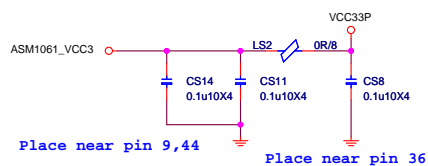


1.2V delay from 3.3V 90% > 0ms



ASM1061 POWER Consumption

	3.3V	1.2V	Power (mW)
Idle (mA)	98.45	212.3	579.645
Busy (mA)	91.1	330.7	697.47



Add- 2011.3.18

SATA_SPI_DO don't need pull up (integrated pull-up)
or pull down for Asmedia recommendation.
Asmedia suggest that we use spinup by s/w mode for MB or PCI-E Card.

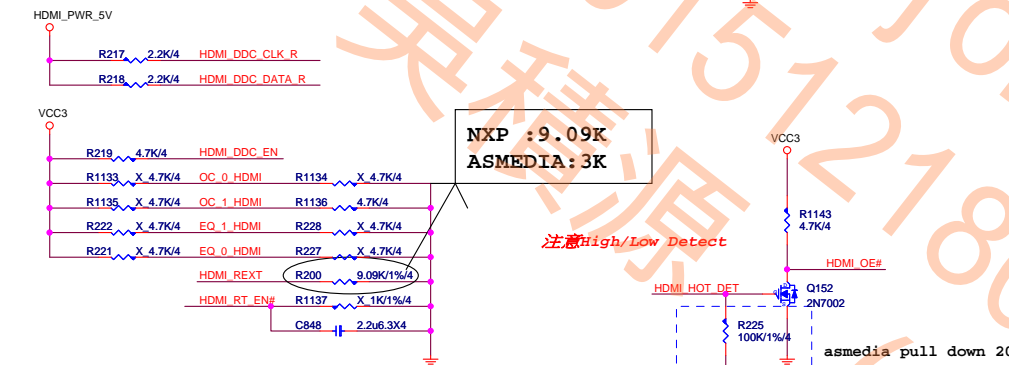
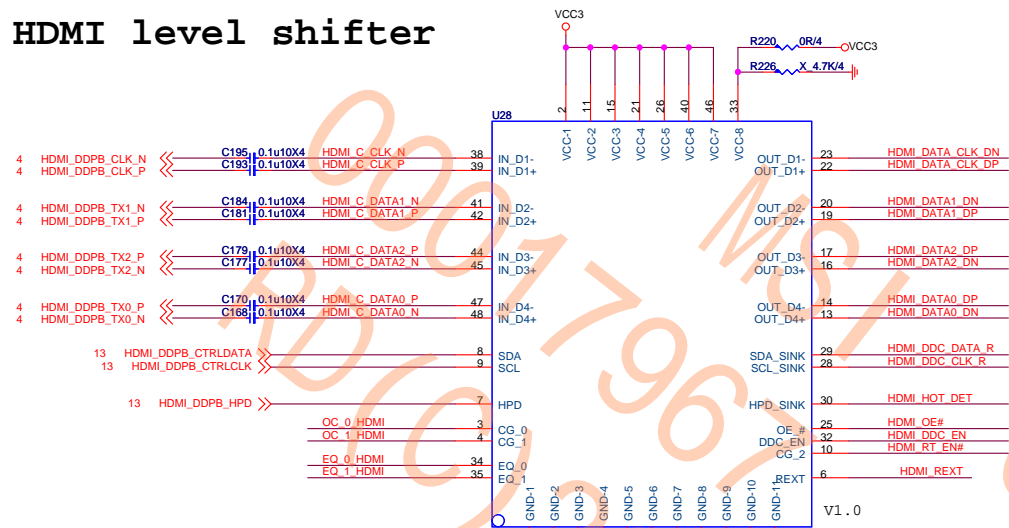


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HDMI level shifter



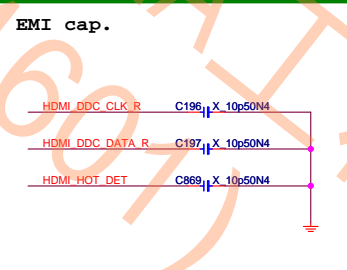
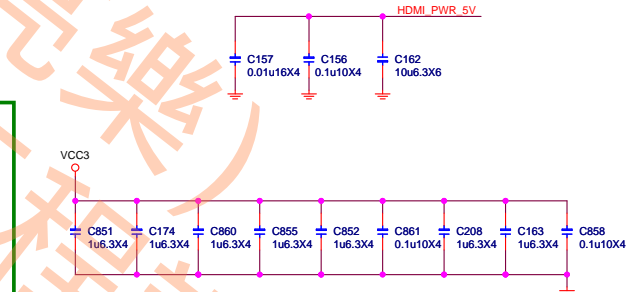
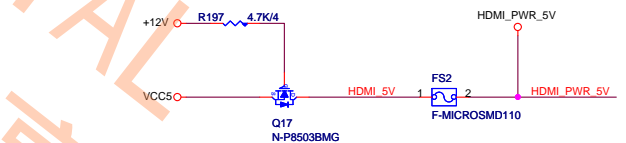
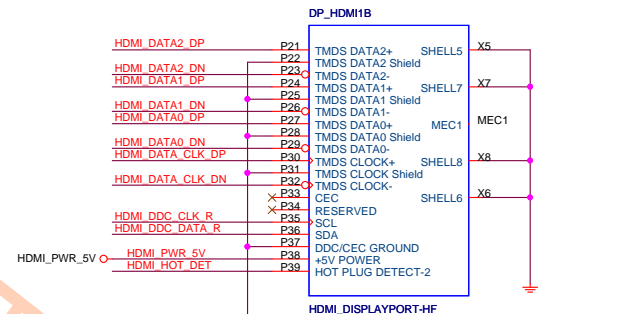
	"0"	"1"
DDC_EN	DDC level shifter disable	DDC level shifter enable
RT_EN#	Input 50 ohm termination resistor enable	the input termination ; resistors are set to high impedances
OE#	enable	the chip is power down and input termination resistors will be at high impedance.
HPD_SINK	disable	enable
DDCBUF_EN	For DDC level shifting configuration, please refer to Table.	
REXT		

[DDC_EN, DDCBUF_EN, OE#]	DDC Passive Switch	DDC Active Buffer
1, 0, X	On	Off
1, 1, 0	Off	On
1, 1, 1	Off	Off
0, X, X	Off	Off

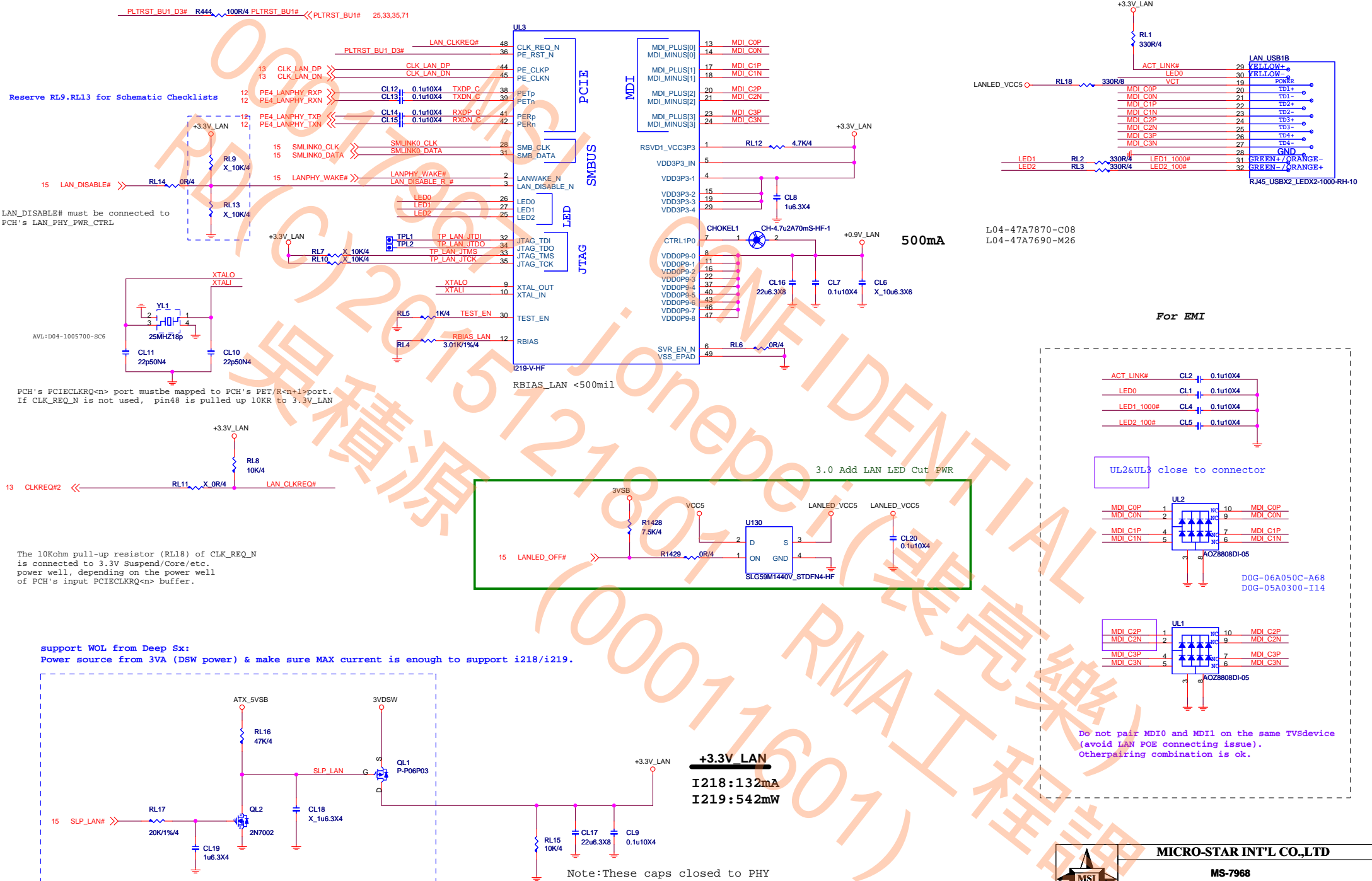
PC1, PC0		note
00	8 dB	internal pull-down at ~500K ohm.
01	4 dB	
10	12 dB	
11	0 dB	

Table 8-1. PCH PCI Express Tx/RX - HDMI Signal Mappings

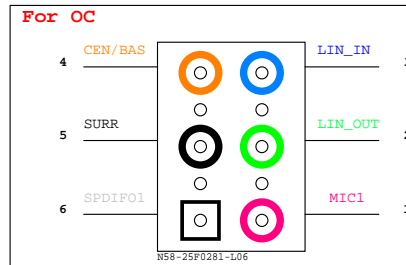
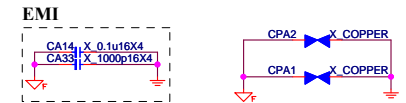
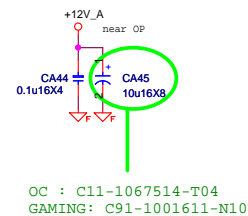
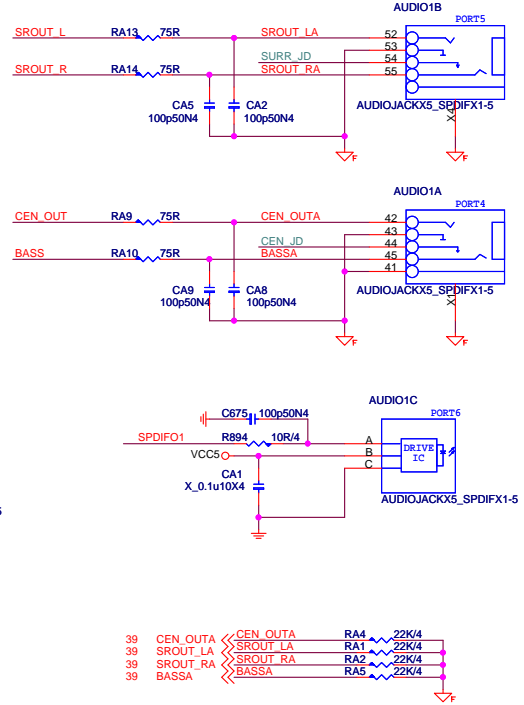
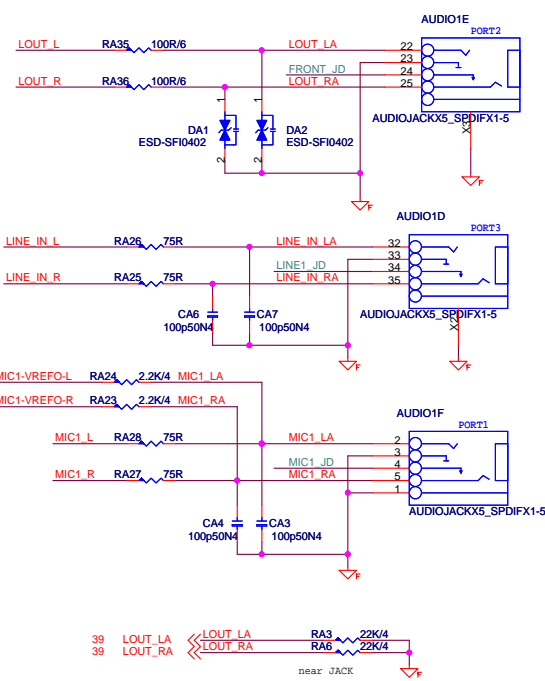
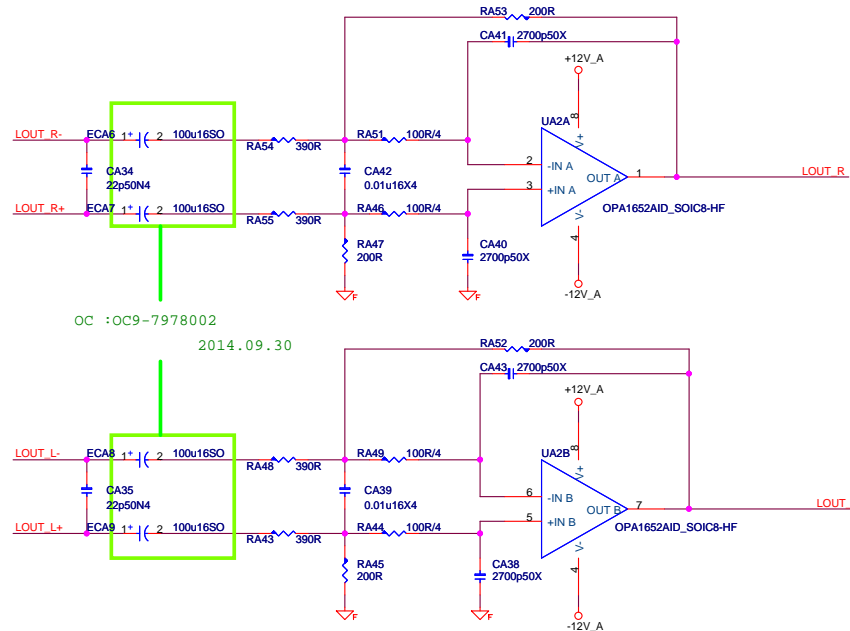
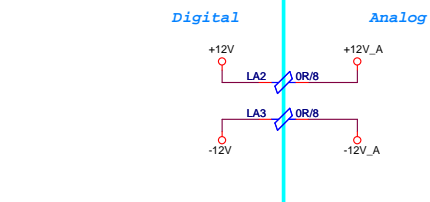
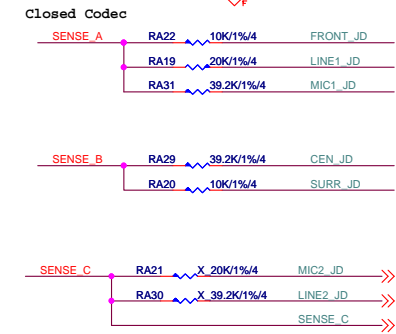
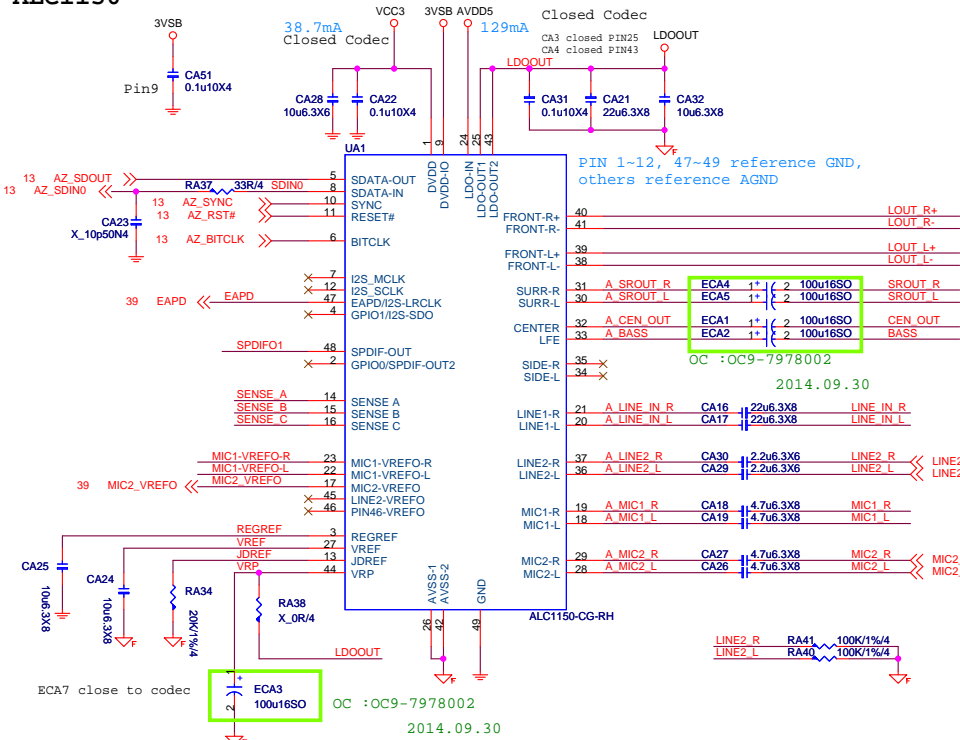
Port	Digital Display Interface Differential Pairs	HDMI Signals	PCH Digital Display Interface Pins
Port B	DDSP_B_TX0_DN	TMDSB_DATA2#	DDPB_ON
	DDSP_B_TX0_DP	TMDSB_DATA2	DDPB_OP
	DDSP_B_TX1_DN	TMDSB_DATA1#	DDPB_1N
	DDSP_B_TX1_DP	TMDSB_DATA1	DDPB_1P
	DDSP_B_TX2_DN	TMDSB_DATA0#	DDPB_2N
	DDSP_B_TX2_DP	TMDSB_DATA0	DDPB_2P
	DDSP_B_TX3_DN	TMDSB_CLK#	DDPB_3N
	DDSP_B_TX3_DP	TMDSB_CLK	DDPB_3P
	DDPB_HPD	DDSP_B_HPD0	Hot plug detect used by HDMI Port B.
	SDVO_CTRLCLK	HDMIB_CTRL_CLK	HDMI DDC lines for Port B
	SDVO_CTRLDATA	HDMIB_CTRL_DATA	



Intel I219V / I218V PHY



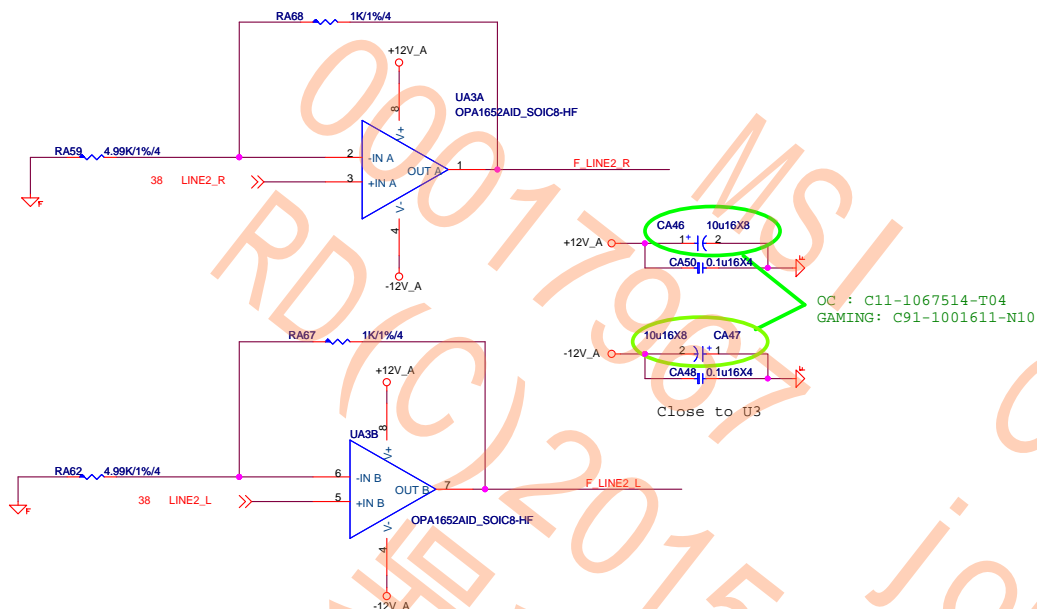
ALC1150



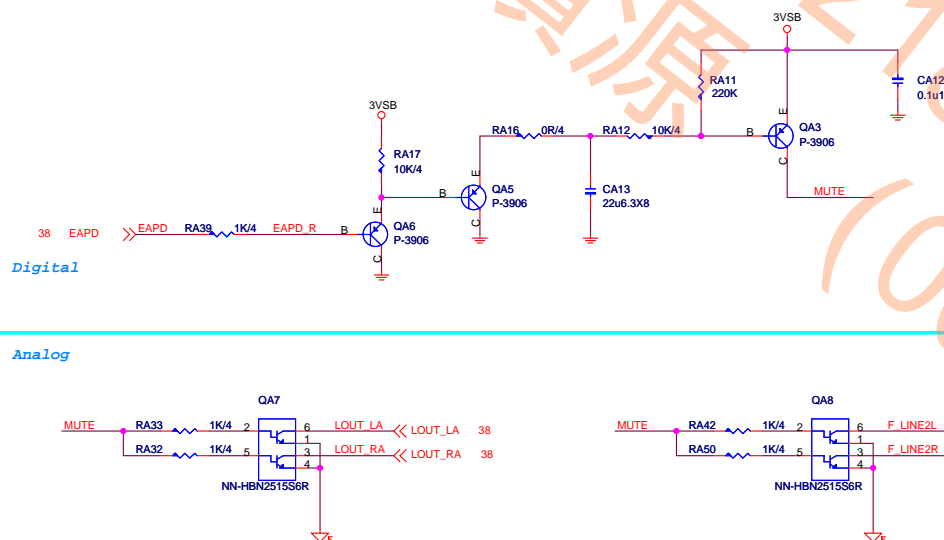
MICRO-STAR INT'L CO.,LTD

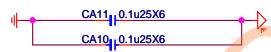
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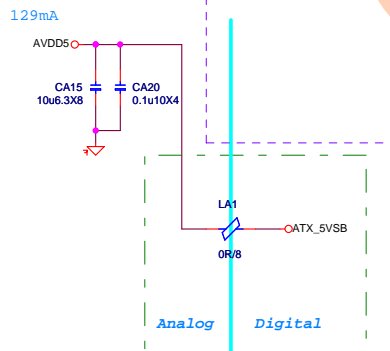
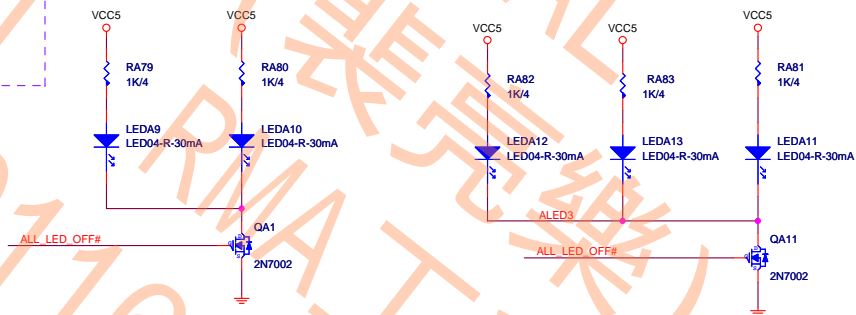
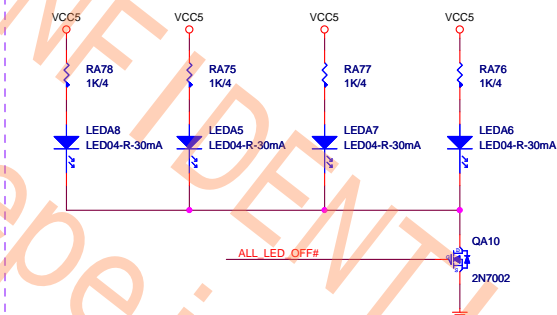
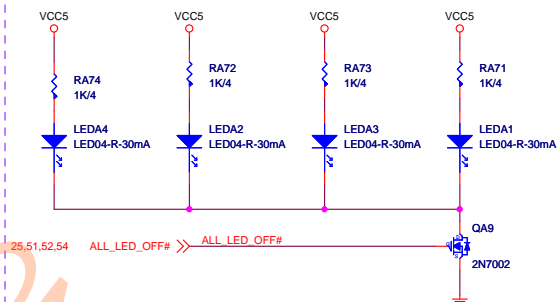
Rear Line OUT De-POP circuit
(De-pop circuit for Rear Line out & Front Headphone out)



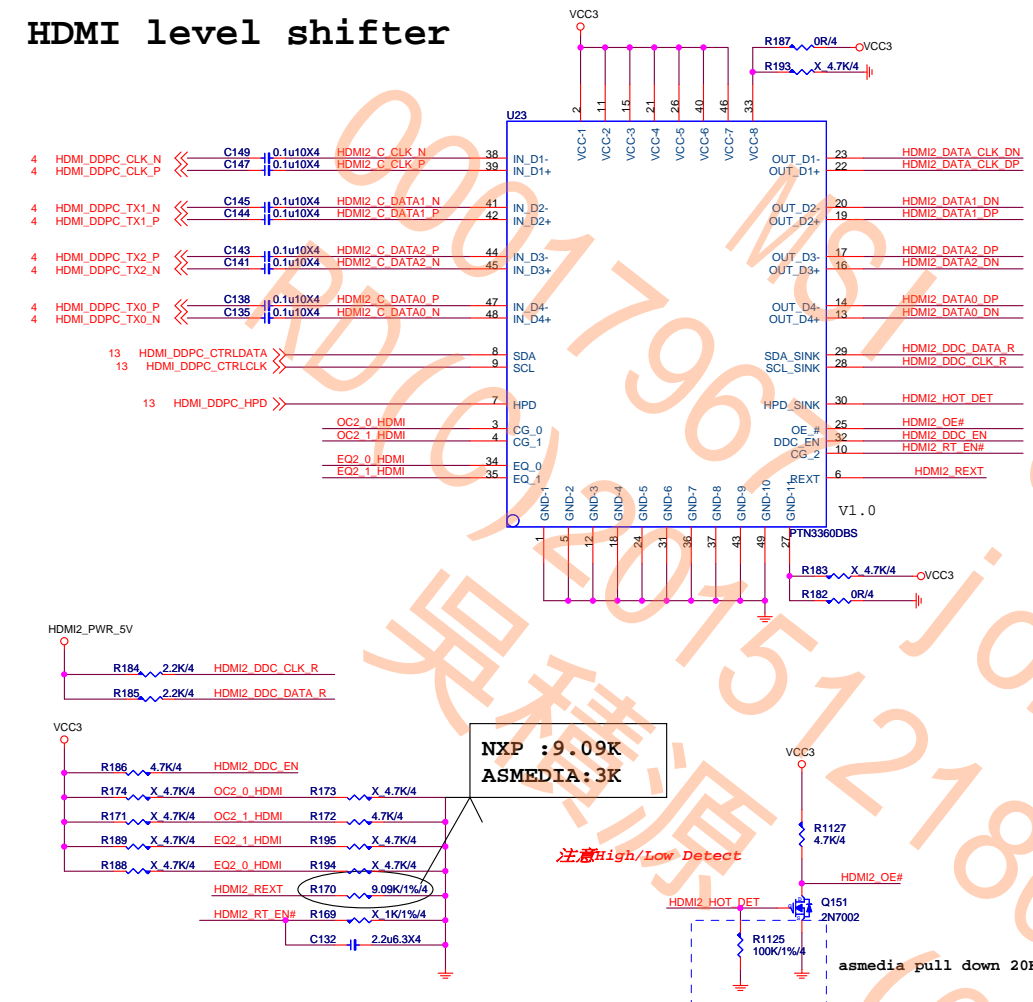


By FAR 10.14

Audio moat is transparent and width 40mil



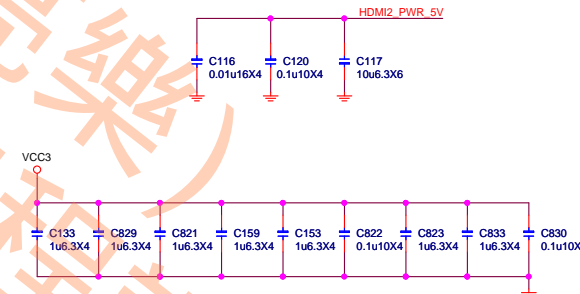
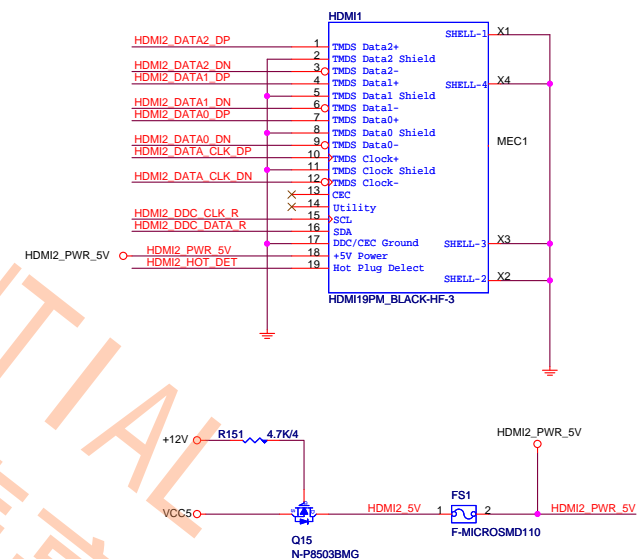
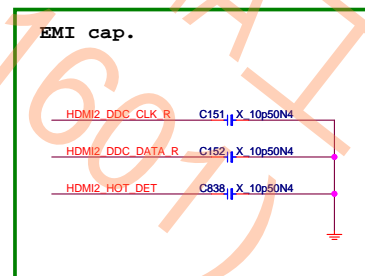
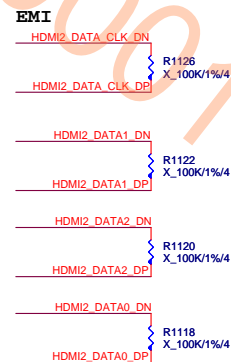
HDMI level shifter



	"0"	"1"
DDC_EN	DDC level shifter disable	DDC level shifter enable
RT_EN#	Input 50 ohm termination resistor enable	the input termination ; resistors are set to high impedances
OE#	enable	the chip is power down and input termination resistors will be at high impedance.
HPD_SINK	disable	enable
DDCBUF_EN	For DDC level shifting configuration, please refer to Table.	
REXT		

[DDC_EN, DDCBUF_EN, OE#]	DDC Passive Switch	DDC Active Buffer
1, 0, X	On	Off
1, 1, 0	Off	On
1, 1, 1	Off	Off
0, X, X	Off	Off

pull-down		note
PC1, PC0		
00	8 dB	internal pull-down at ~500K ohm.
01	4 dB	
10	12 dB	
11	0 dB	



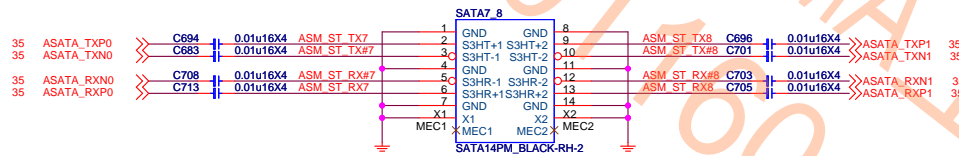
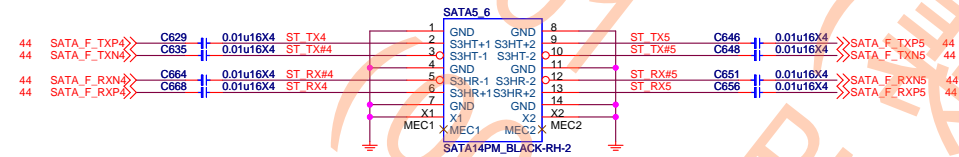
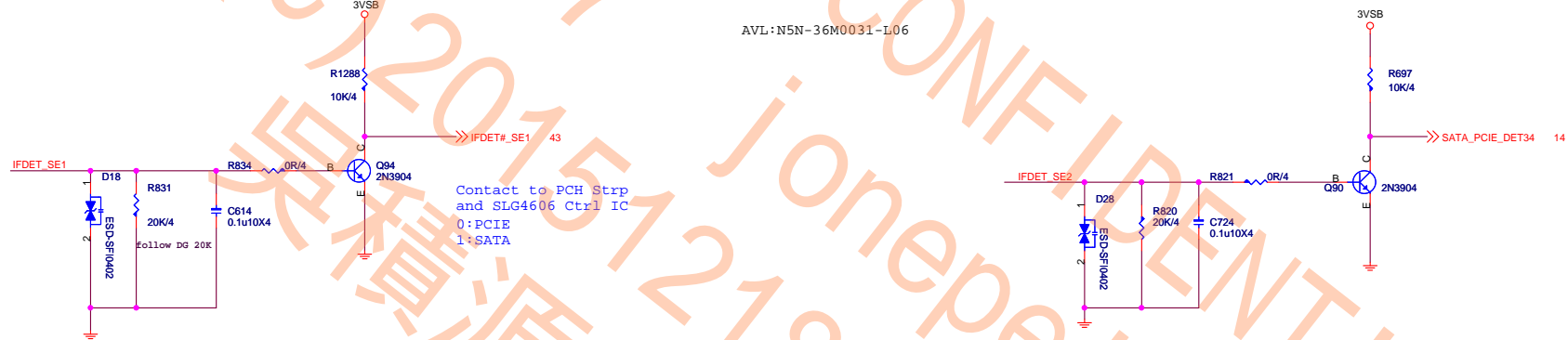
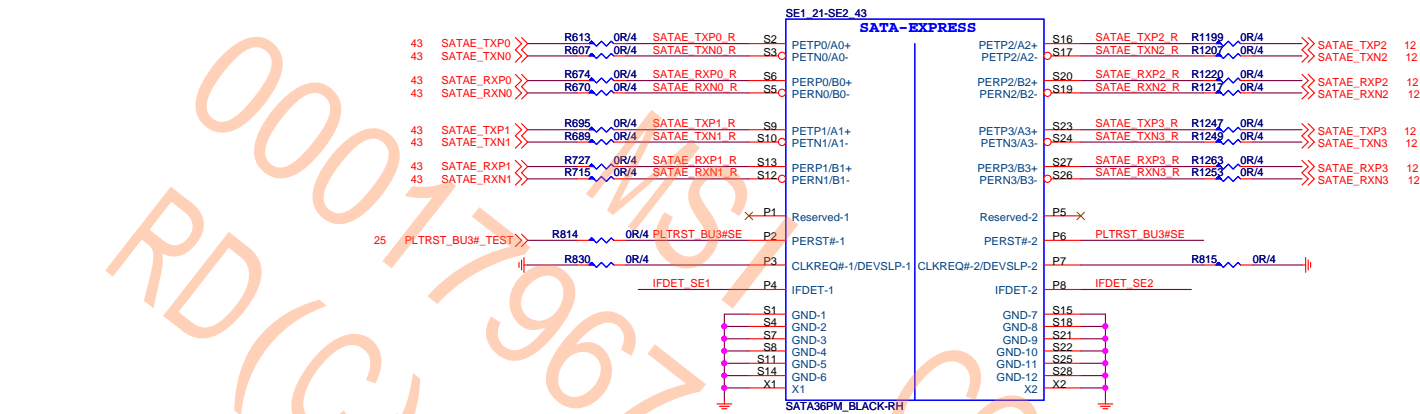
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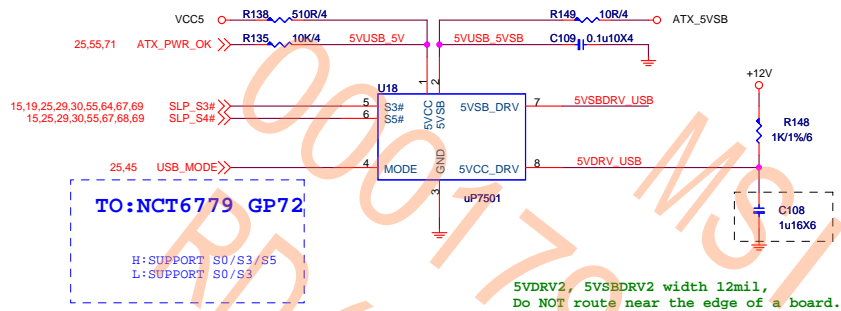
Size Custom	Document Description HDMI2 1.4-PTN3360D	Re 3
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Table 8-1. PCH PCI Express Tx/RX - HDMI Signal Mappings

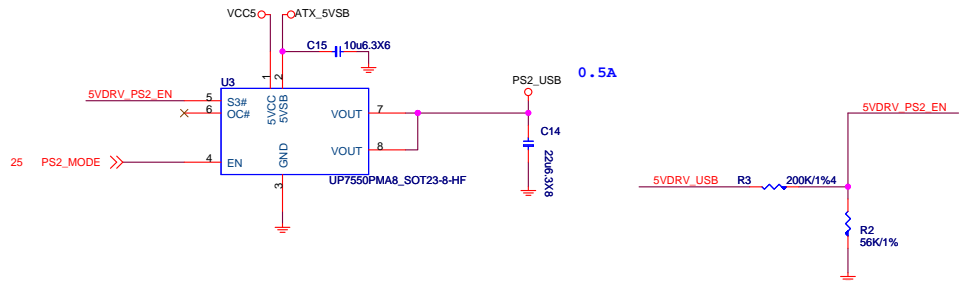
Port	Digital Display Interface Differential Pairs	HDMI Signals	PCH Digital Display Interface Pins
Port B	DDSP_B_TX0_DN	TMDSB_DATA2#	DDPB_0N
	DDSP_B_TX0_DP	TMDSB_DATA2	DDPB_0P
	DDSP_B_TX1_DN	TMDSB_DATA1#	DDPB_1N
	DDSP_B_TX1_DP	TMDSB_DATA1	DDPB_1P
	DDSP_B_TX2_DN	TMDSB_DATA0#	DDPB_2N
	DDSP_B_TX2_DP	TMDSB_DATA0	DDPB_2P
	DDSP_B_TX3_DN	TMDSB_CLK#	DDPB_3N
	DDSP_B_TX3_DP	TMDSB_CLK	DDPB_3P
	DDPB_HPD	DDSP_B_HPD0	Hot plug detect used by HDMI Port B.
	SDVO_CTRLCLK	HDMI0_CTRL_CLK	HDMI DDC lines for Port B
SDVO_CTRLDATA	HDMI0_CTRL_DATA		



USB POWER

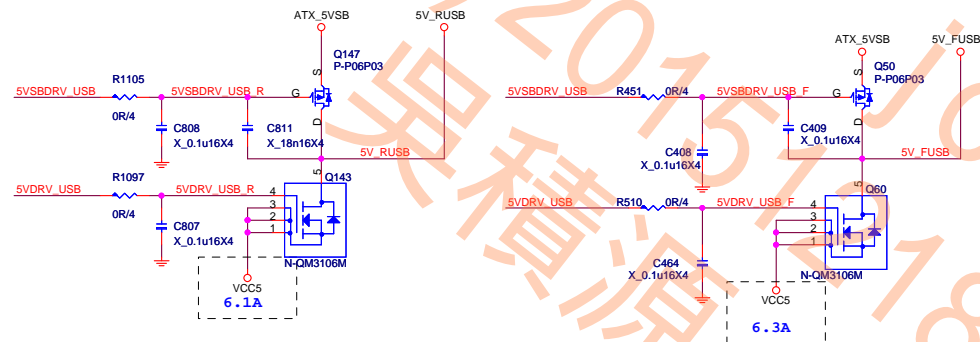


PS2 POWER

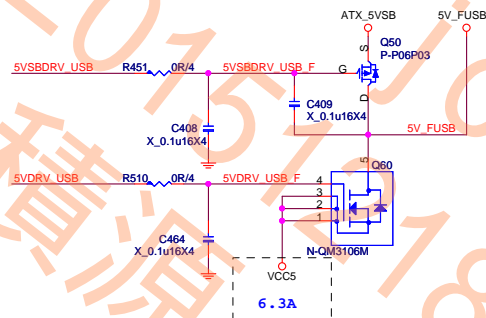


USB MODE

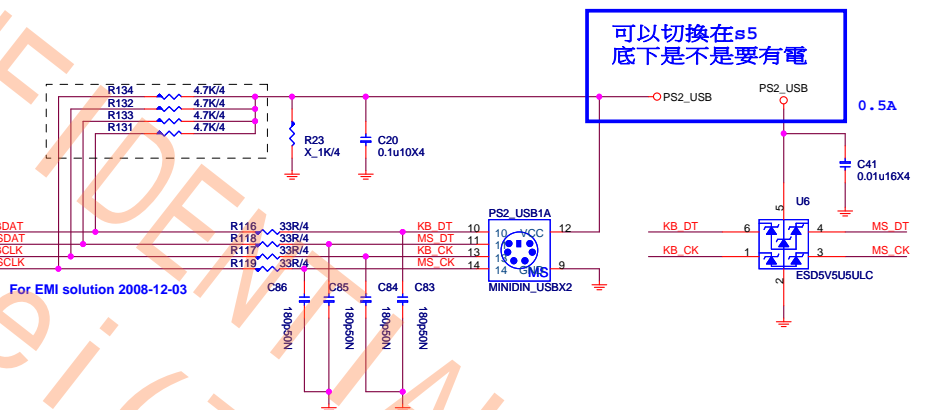
REAR USB PORT POWER



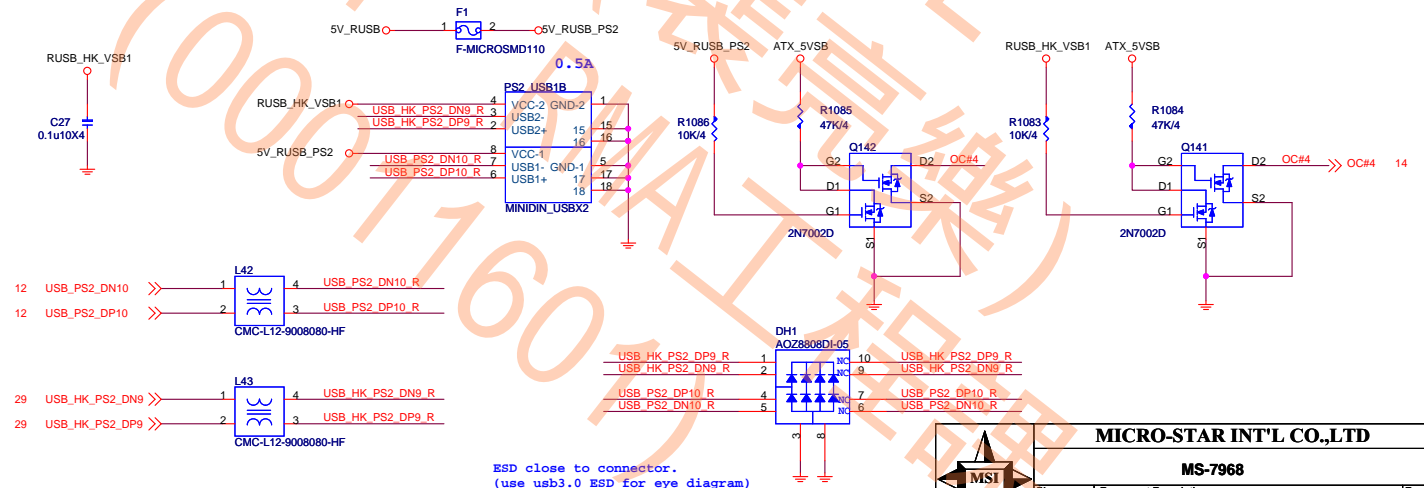
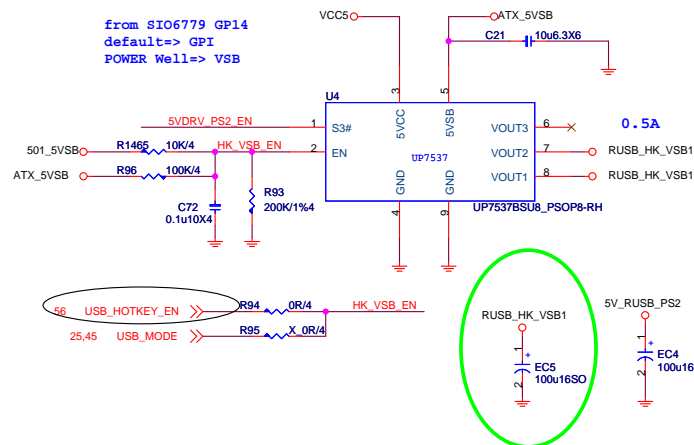
FRONT USB PORT POWER



PS2 KEYBOARD & MOUSE CONNECTOR



REAR USB PORT 8,9 (With PS2)

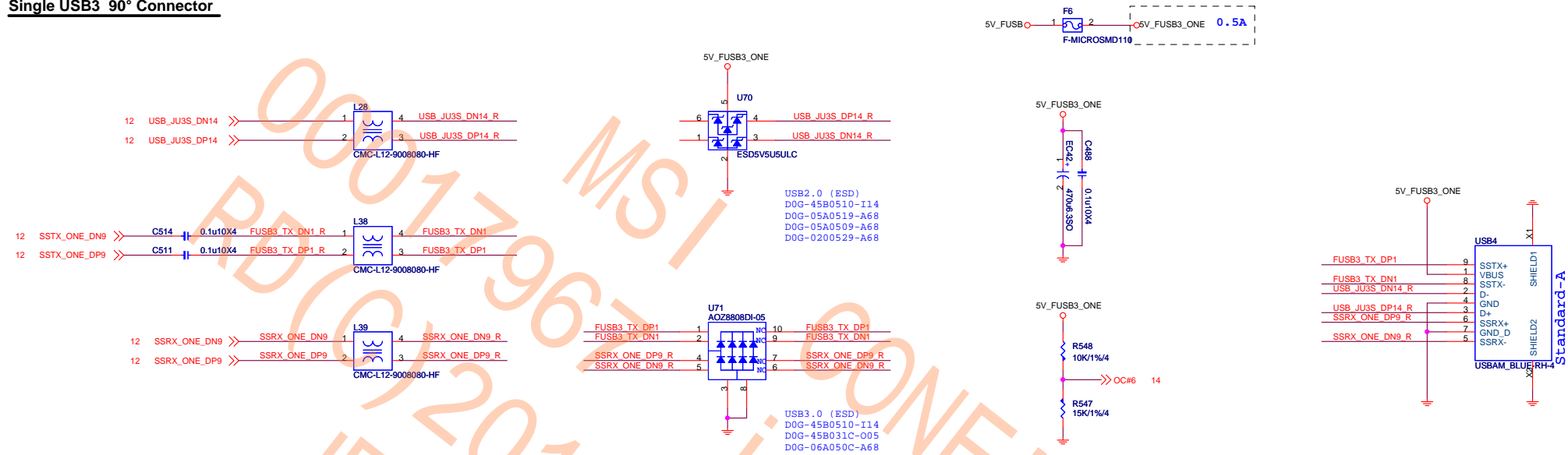


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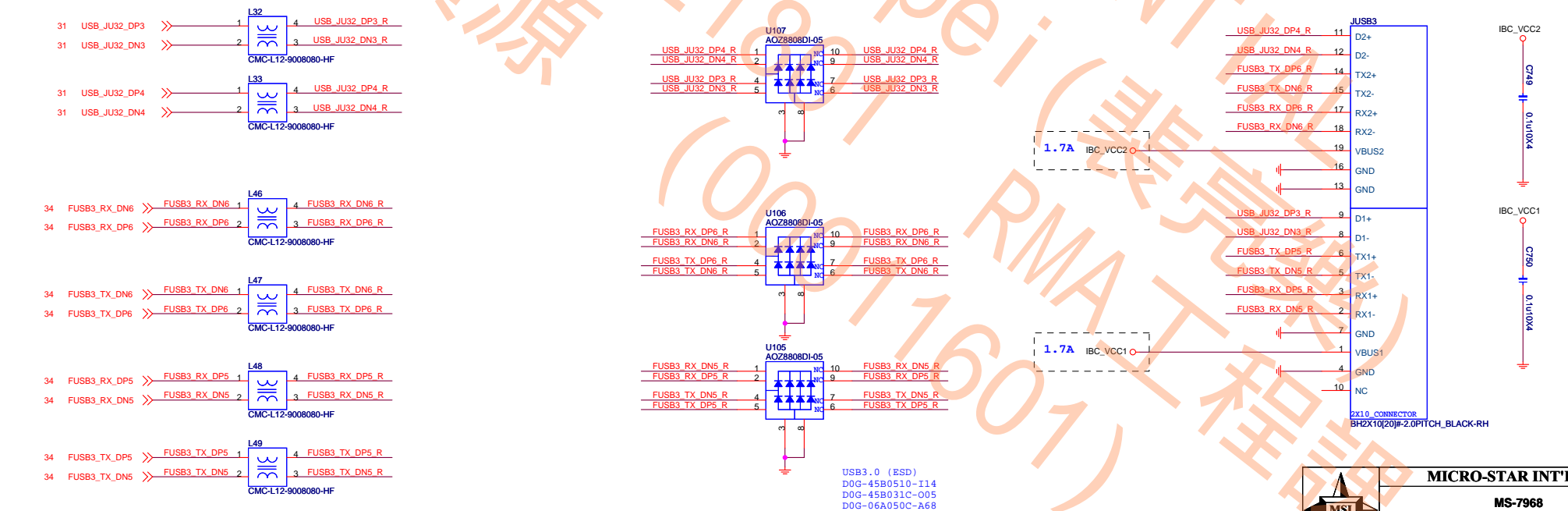
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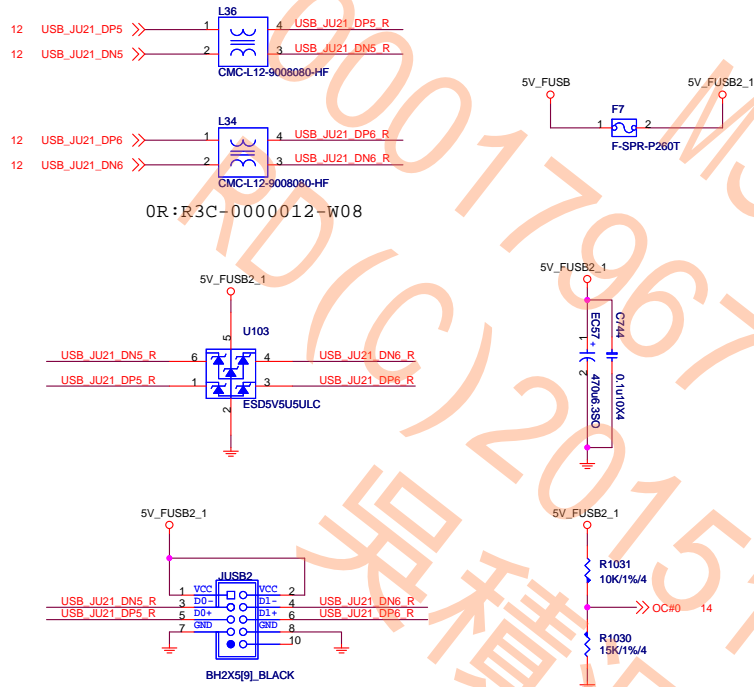
Single USB3 90° Connector



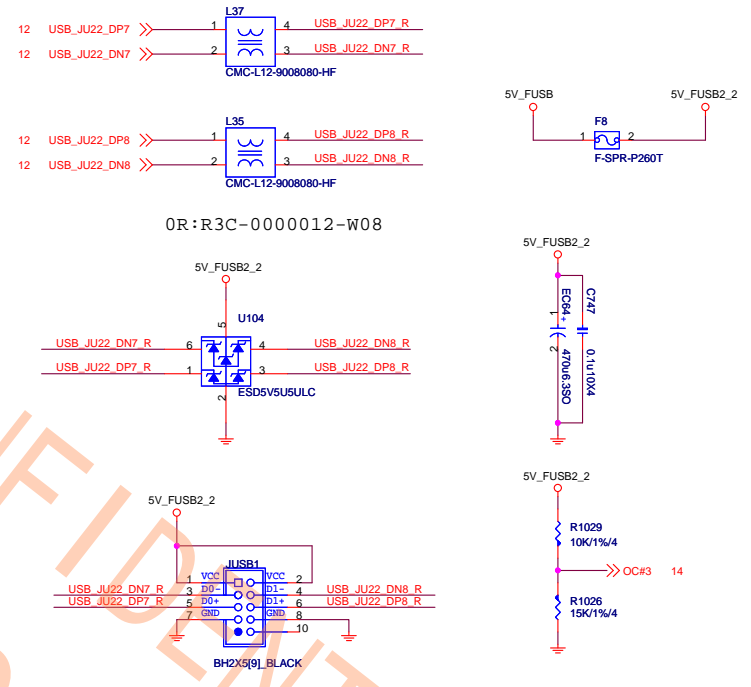
Front USB3 180° BOX Header



FRONT USB PORT 1,2



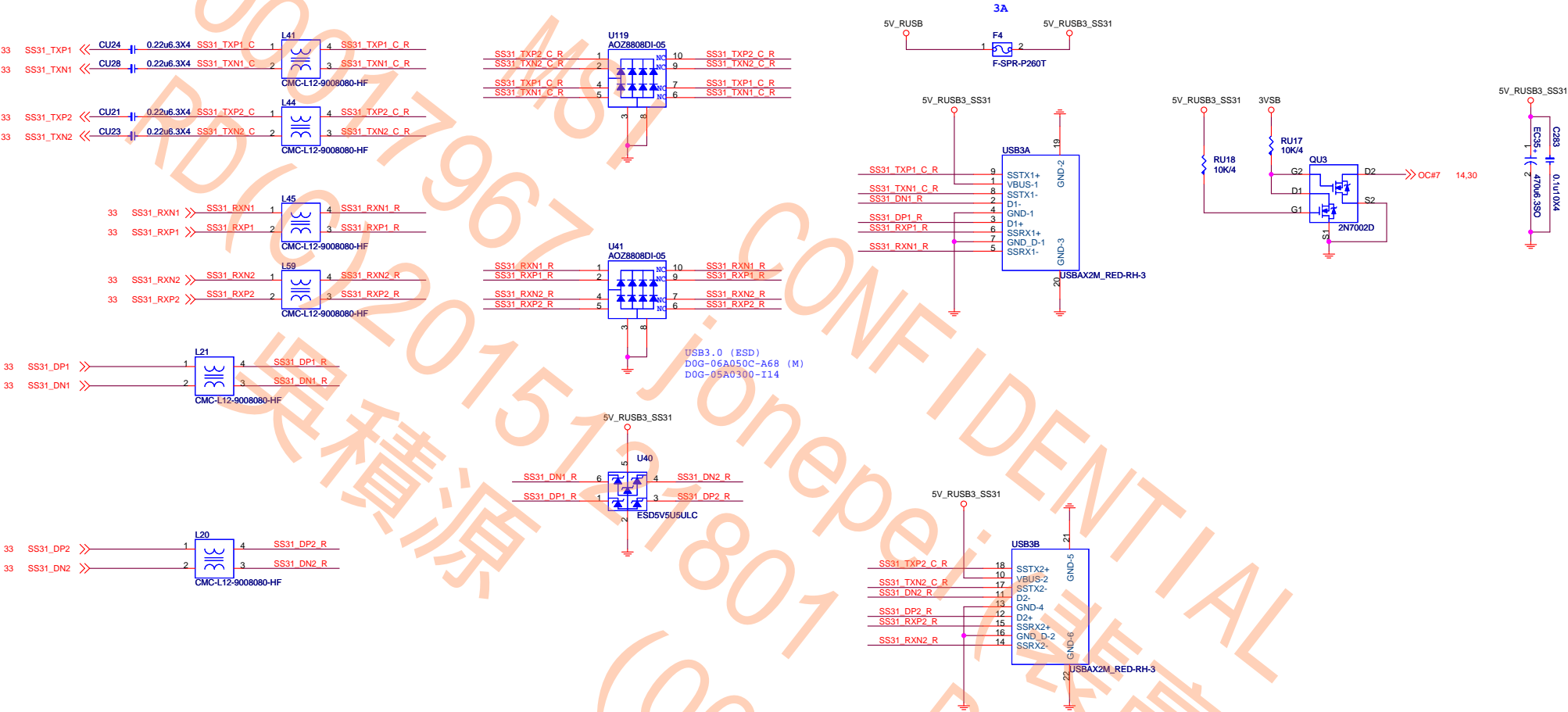
FRONT USB PORT 7,8



Rear USB3.1 Connector

Rear USB3 CONN

Important--
If USB3.0 signal connect to front pin header,
please must less than 0.6 inch, short trace
has better eye diagram with some bad fly cable by SI customer.

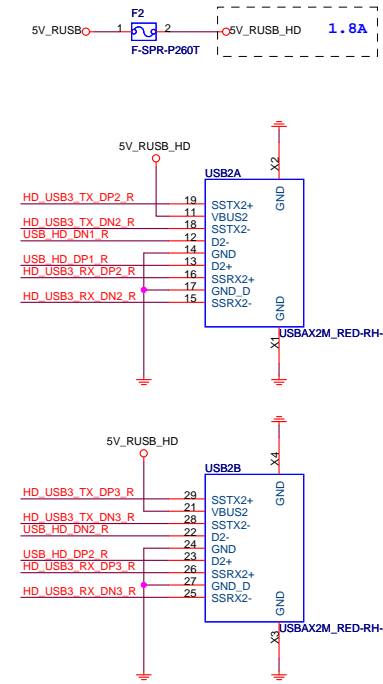
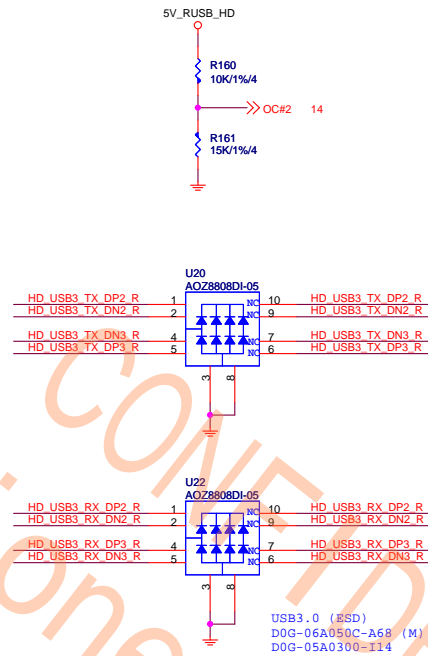
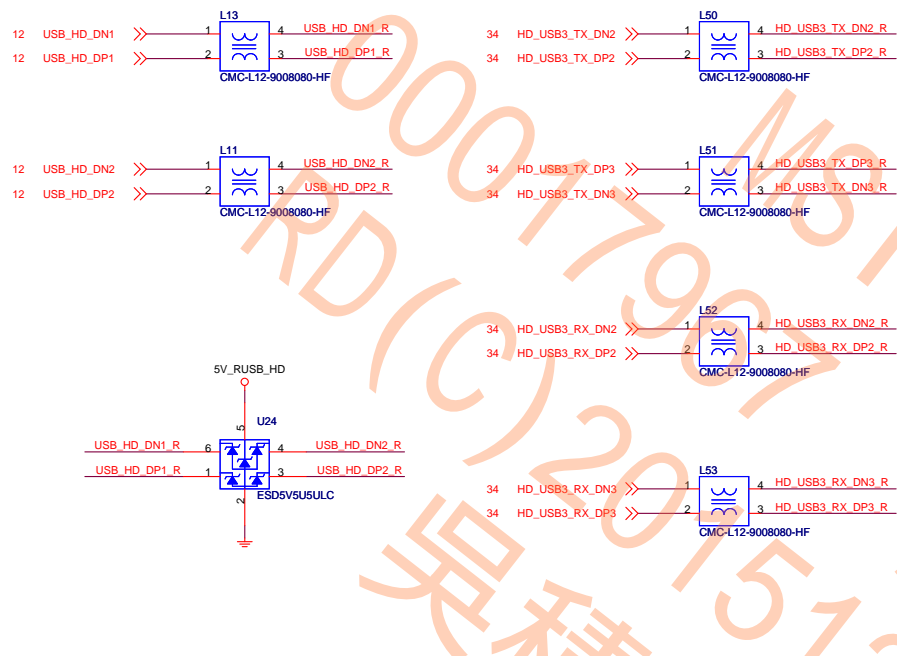


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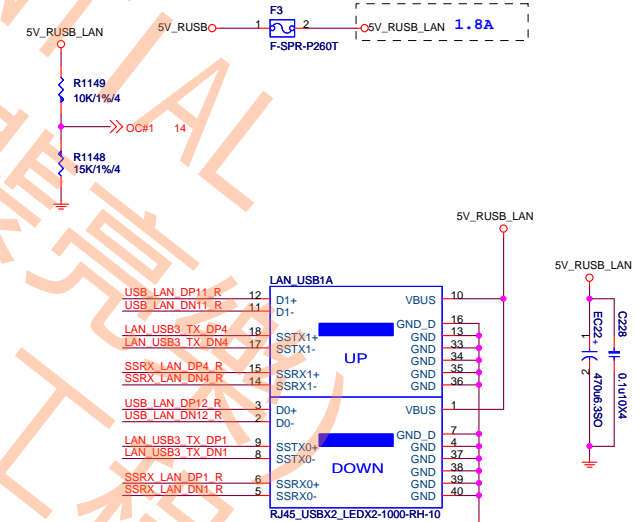
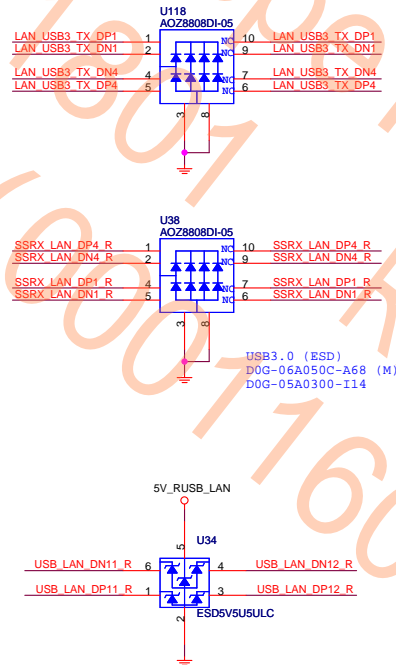
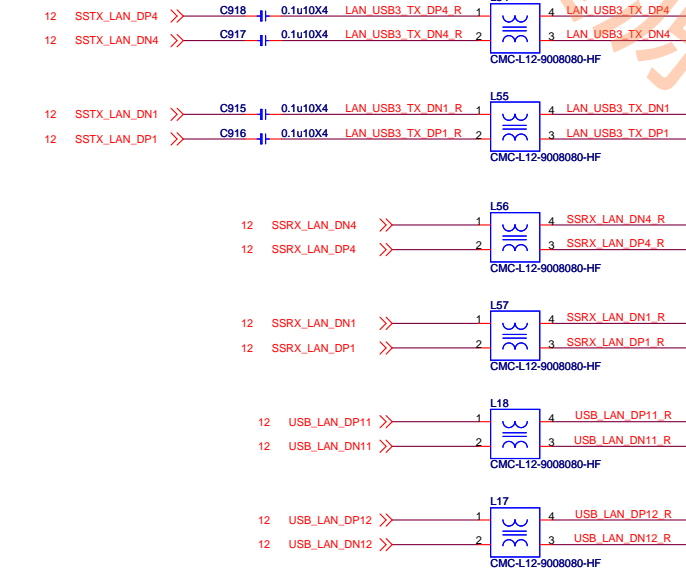
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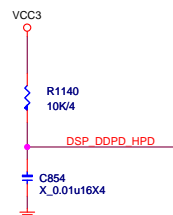
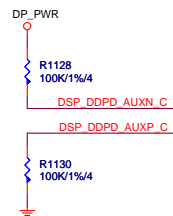
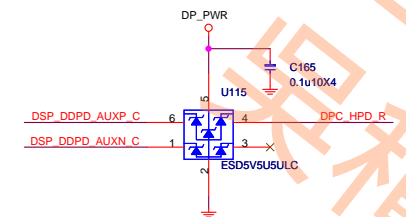
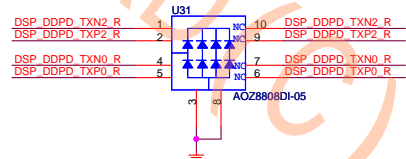
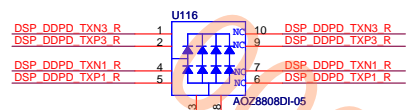
Size	Document Description	Rev
Custom	Rear USB3.1 CONNECTOR	31
Date:	Tuesday, June 30, 2015	Sheet 48 of 77

Rear USB3 (w/ HDMI)

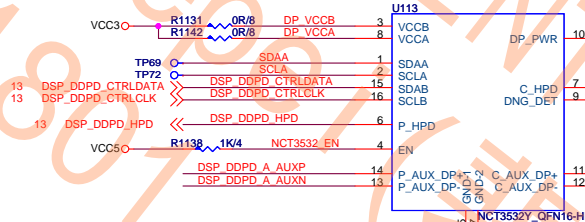
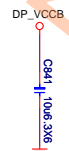


Rear USB3 (w/ LAN)

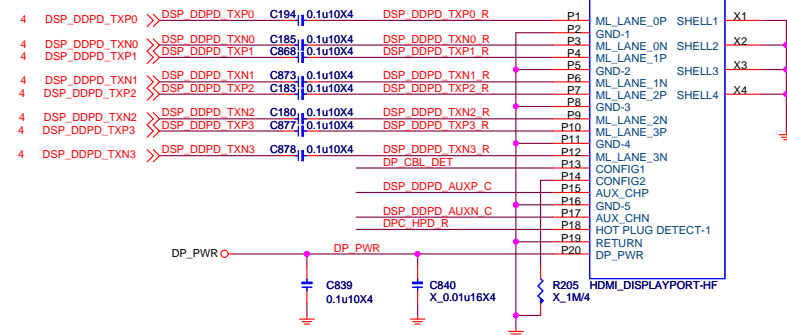




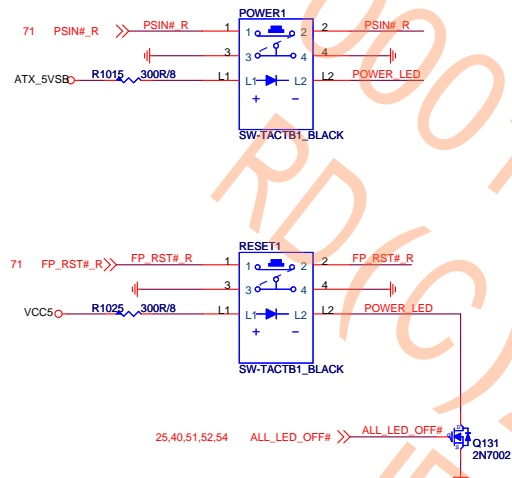
DSP_DDPD_AUXP >> DSP_DDPD_AUXP C843 0.1u10X4 DSP_DDPD_A_AUXP
 DSP_DDPD_AUXN >> DSP_DDPD_AUXN C844 0.1u10X4 DSP_DDPD_A_AUXN



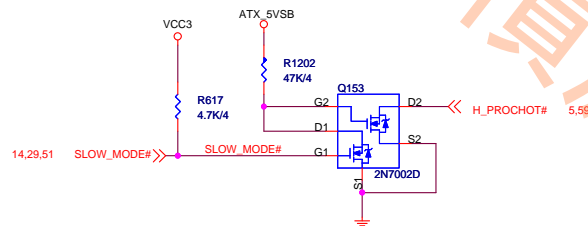
I98-3532Y0C-N62



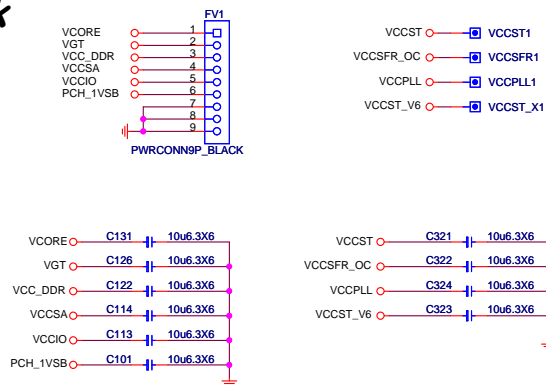
PWR/RST Botton



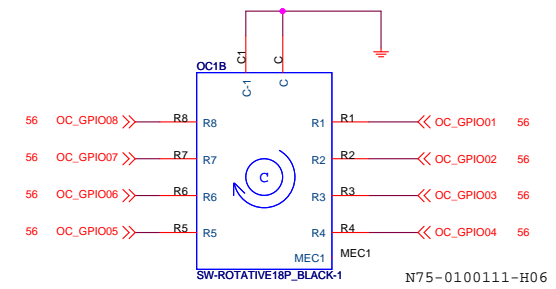
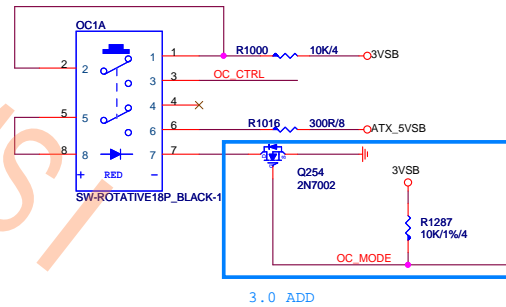
Slow Mode



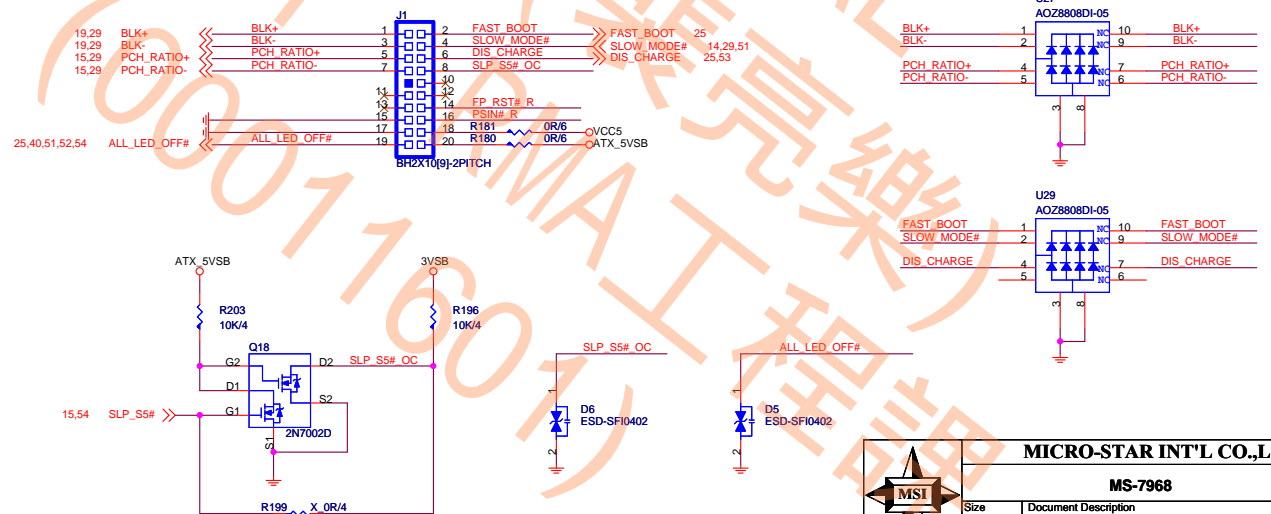
Vcheck



OC Genie

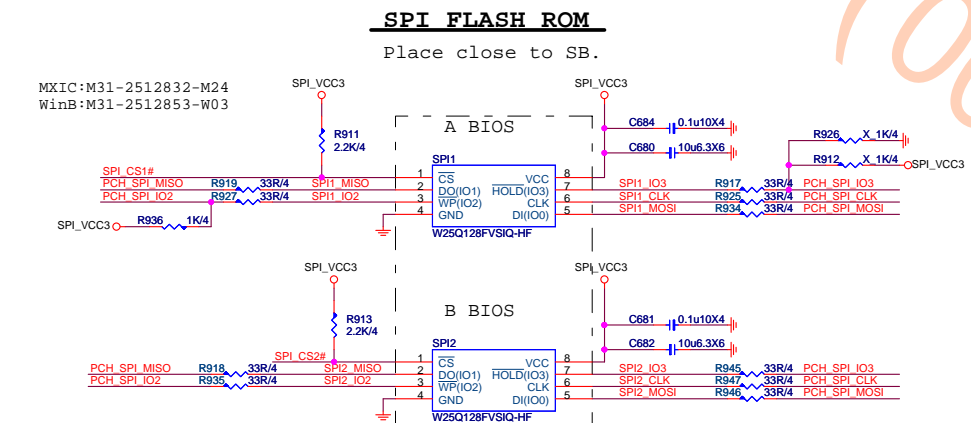
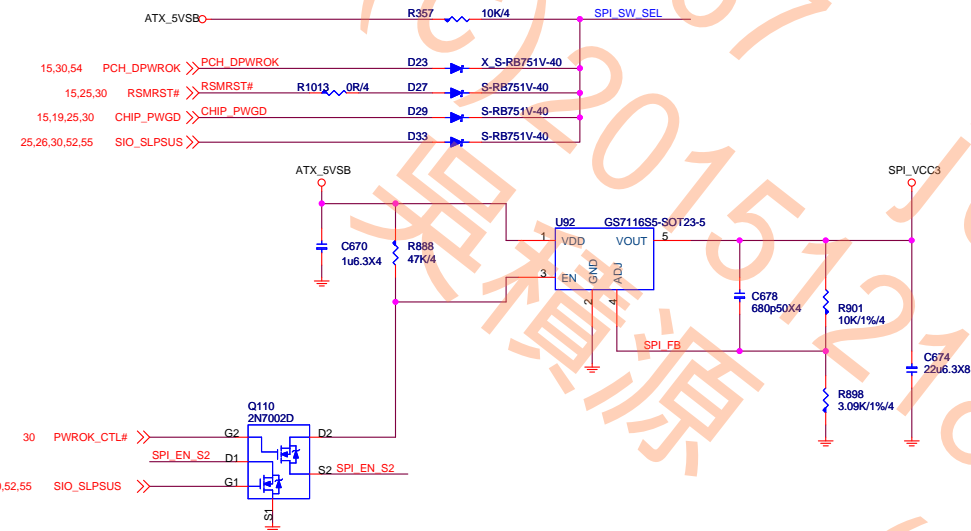
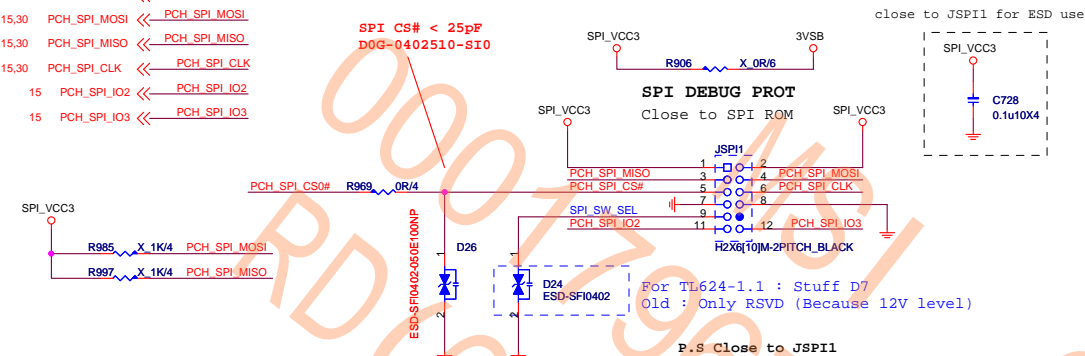


OC DASH Board Pin Header



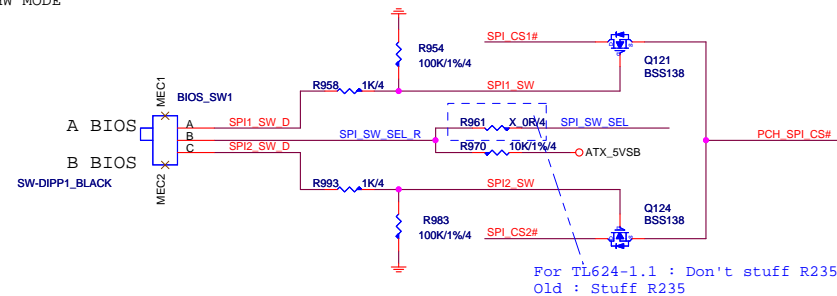
Part Number:N31-2061341-H06

15,30 PCH_SPI_CS0# << PCH_SPI_CS0#
 15,30 PCH_SPI_MOSI << PCH_SPI_MOSI
 15,30 PCH_SPI_MISO << PCH_SPI_MISO
 15,30 PCH_SPI_CLK << PCH_SPI_CLK
 15 PCH_SPI_IO2 << PCH_SPI_IO2
 15 PCH_SPI_IO3 << PCH_SPI_IO3

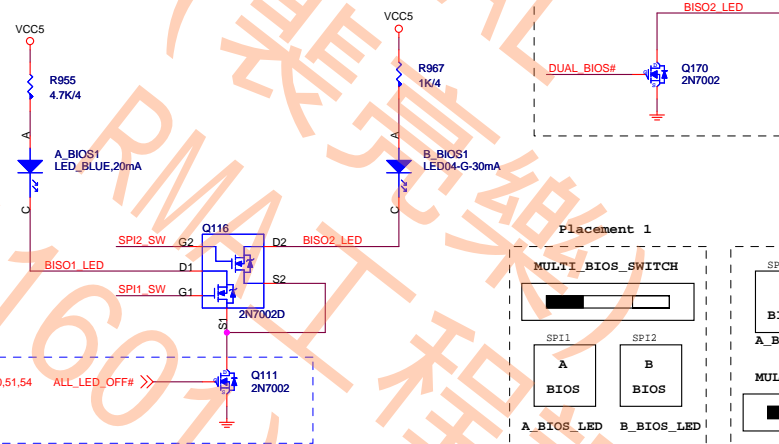
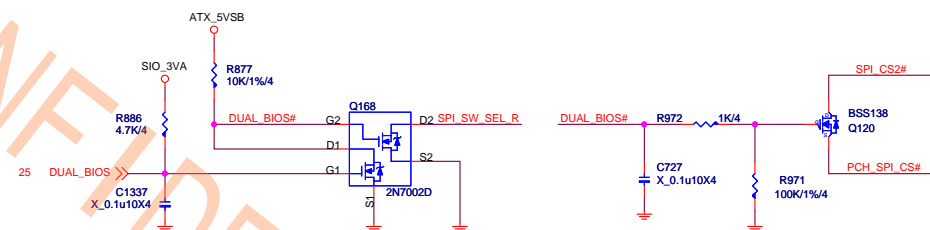


*SPI_CLK & SPI_MOSI must be length matched to within 500mils. < 6 inch
 *SPI_CLK & SPI_CS# must be length matched to within 500mils.

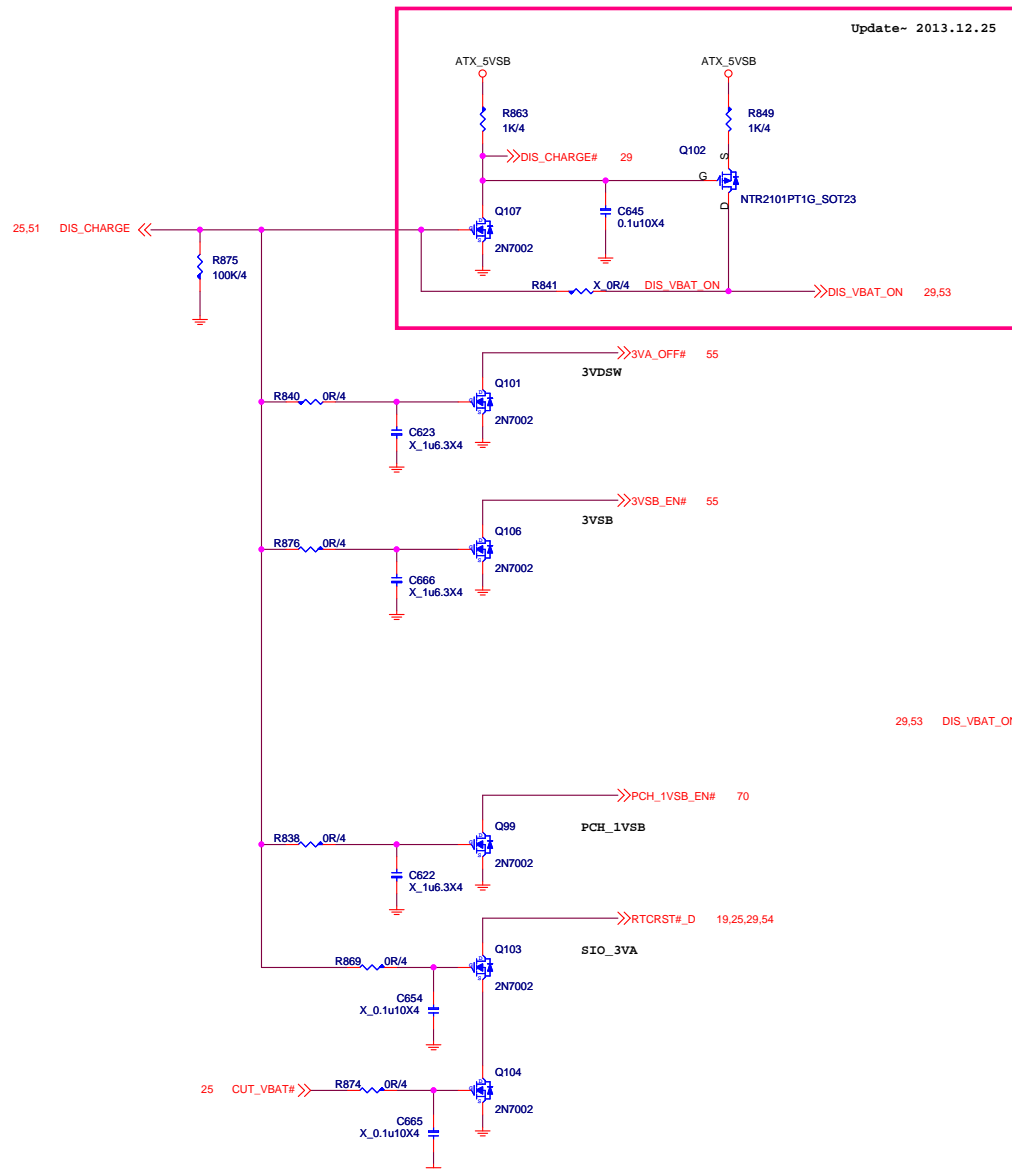
HW MODE



For auto testing in factory.



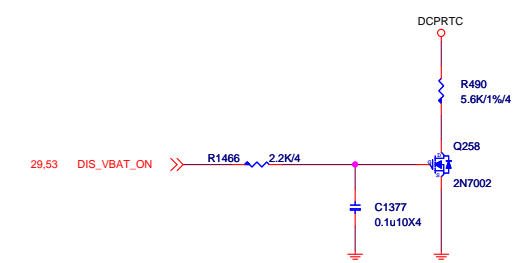
MICRO-STAR INT'L CO.,LTD		
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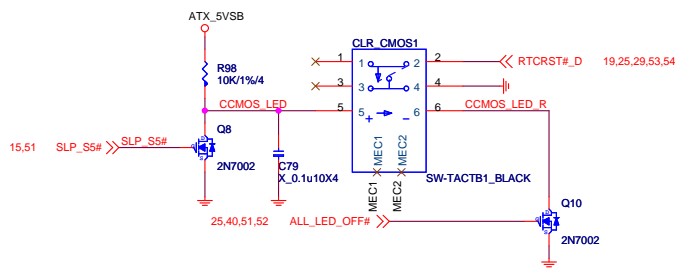
pin header+F75501
pin header only

	R891,R892,Q115,Q114 / R894
O	X
X	O

Add DCRTC discharge circuit



HW MODE

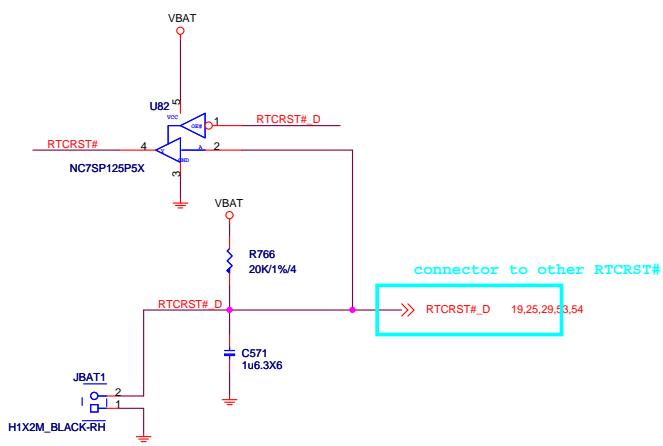
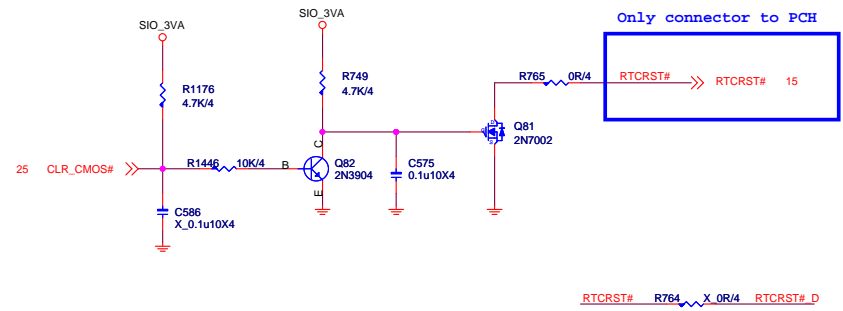


Clear CMOS button

LED LIGHTING RULE

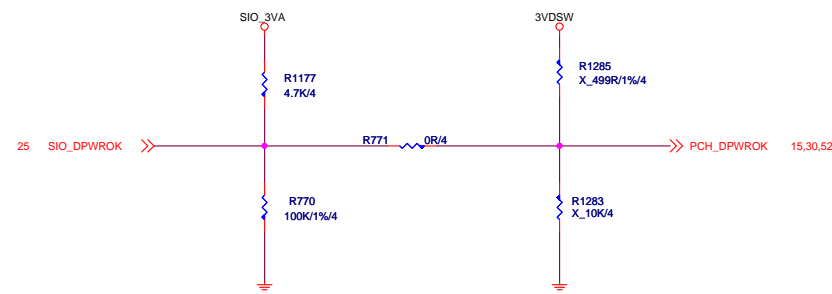
S0/S3/S4 : LED OFF
S5 : LED ON

BIOS MODE

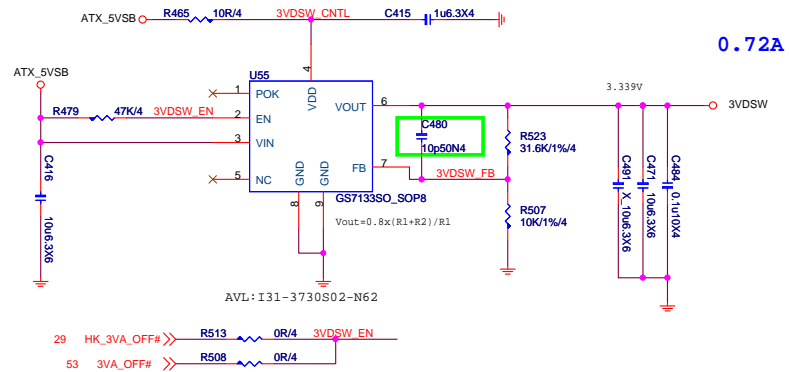


co-lay

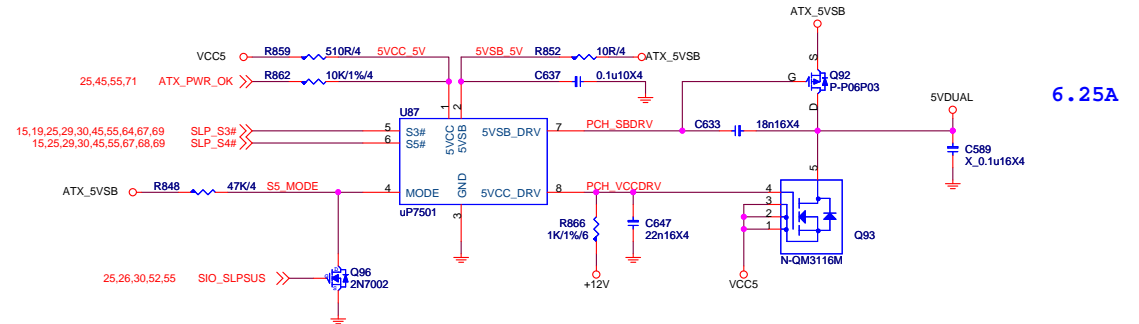
tri-state		
INPUT		outout
PIN1	PIN2	pin4
L	H	H
L	L	L
H	X	Z



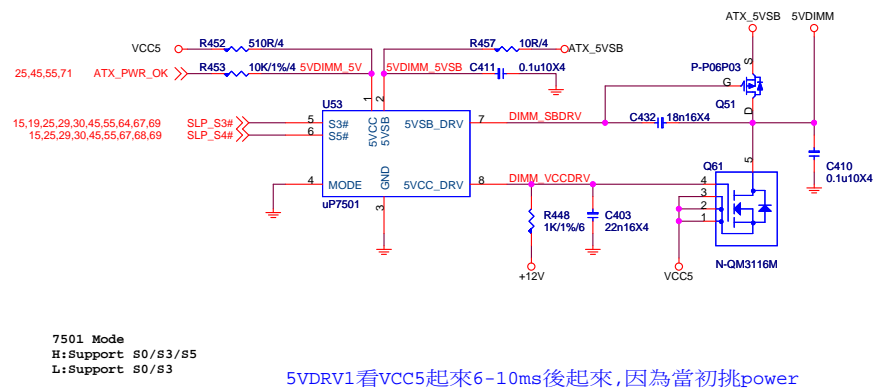
3VDSW



5VDUAL

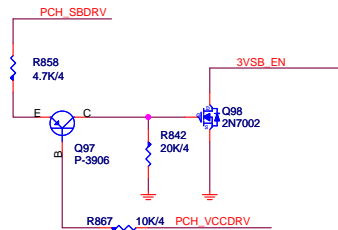
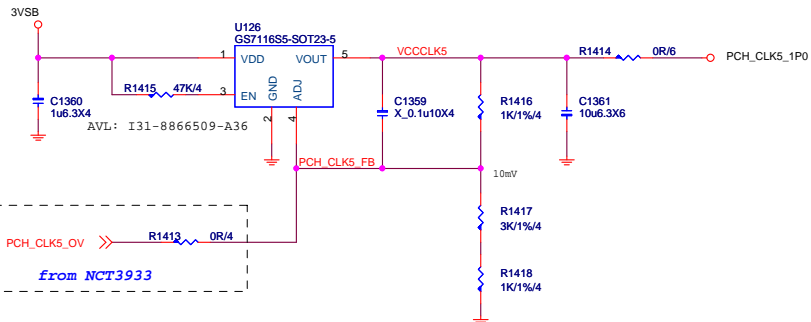
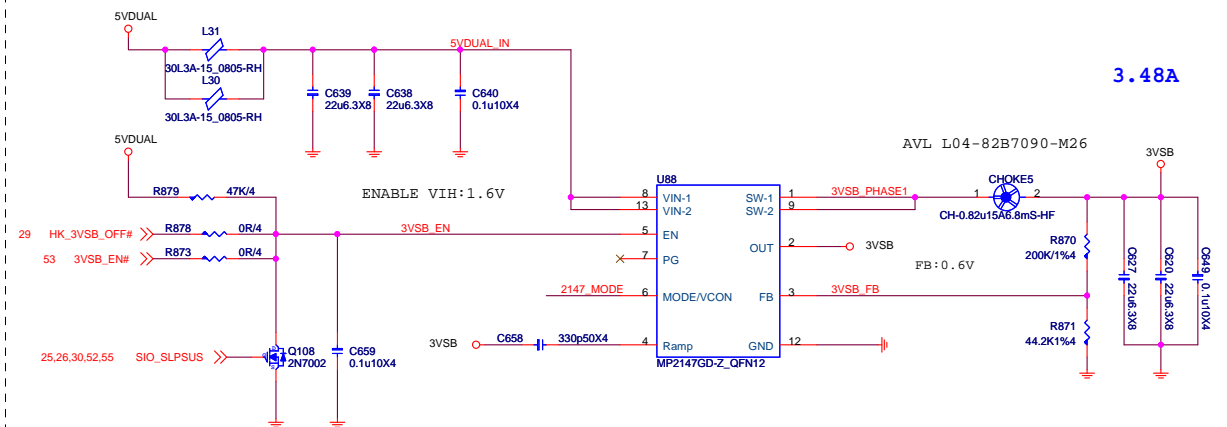


5VDIMM FOR DDR

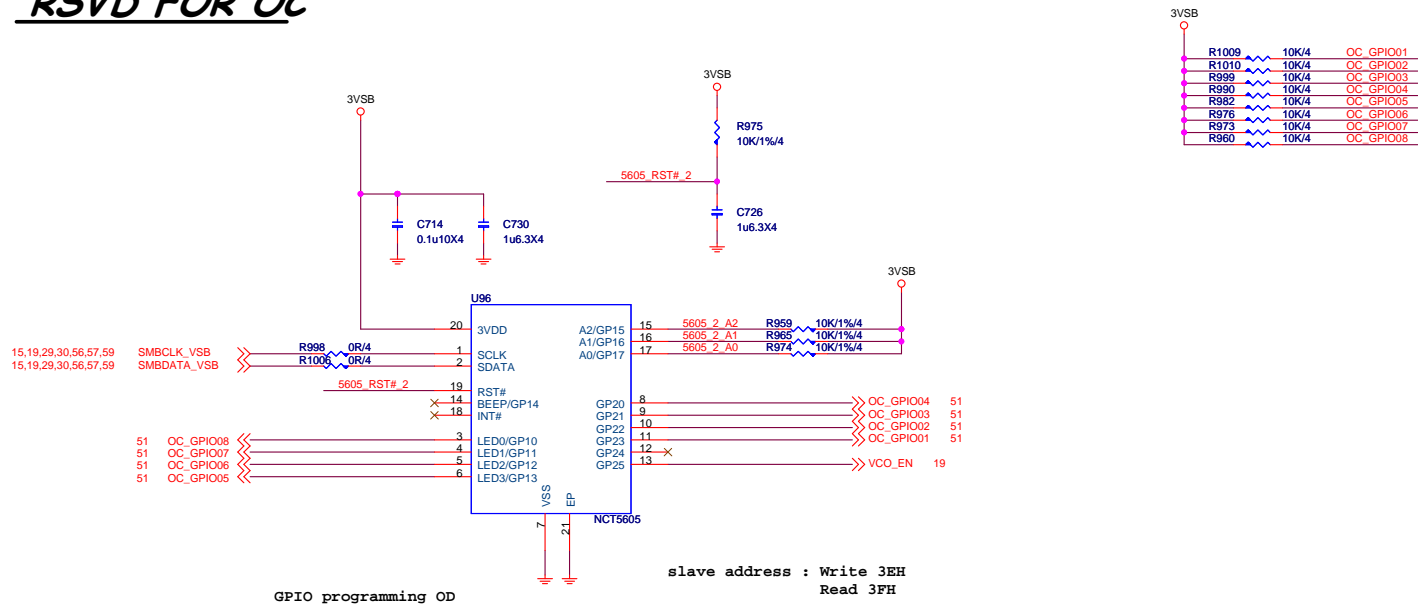
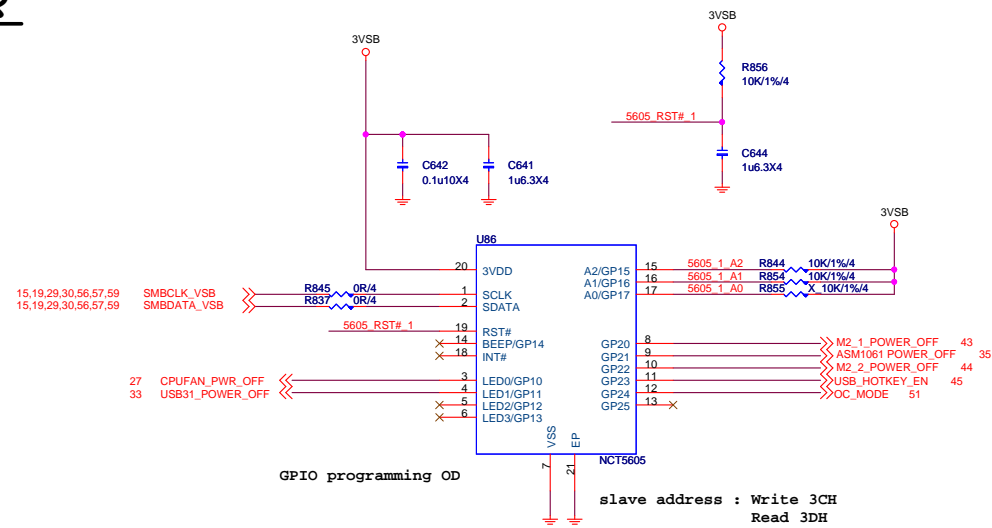


3VSB

for OC & Gaming



防G3-->S5底下5VSBDRV2瞬間有電變沒電,使得下一級電壓爬升有drop

RSVD FOR OC

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Size	Custom
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Document Description
GPIO IC-NCT5605

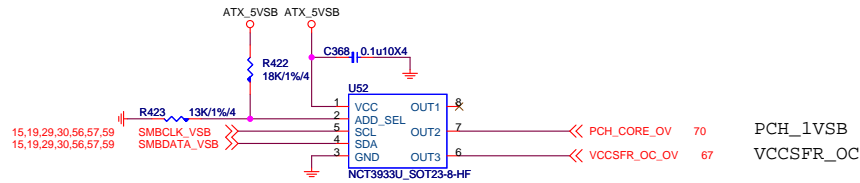
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31

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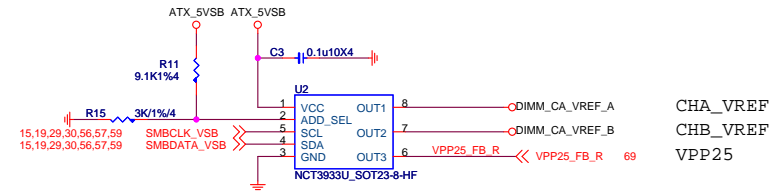
UPI VOLTAGE CONSOLE

0x26:RH=18K,RL=13K



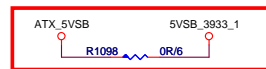
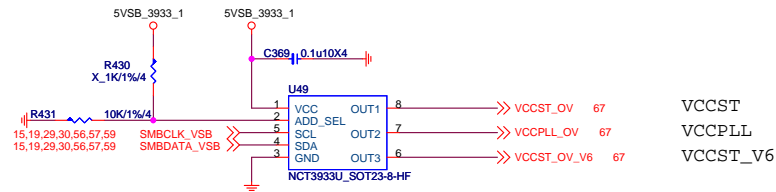
UPI VOLTAGE CONSOLE

0x28:RH=9.1K,RL=3K



UPI VOLTAGE CONSOLE

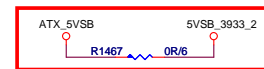
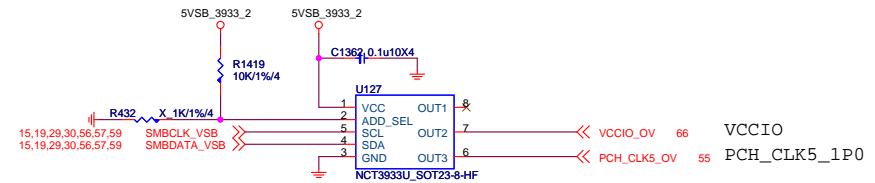
0x2A:RH=9.1K,RL=3K



For VCCST keep Voltage

UPI VOLTAGE CONSOLE

0x20:RH=18K,RL=13K



For VCCIO keep Voltage

UPI VOLTAGE CONSOLE

0x20:RH=10K,RL=OPEN

ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

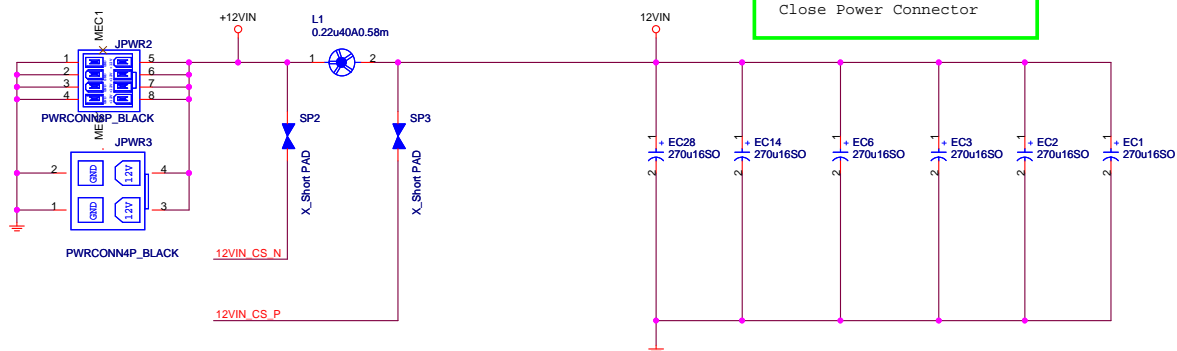
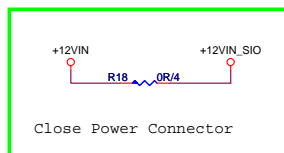
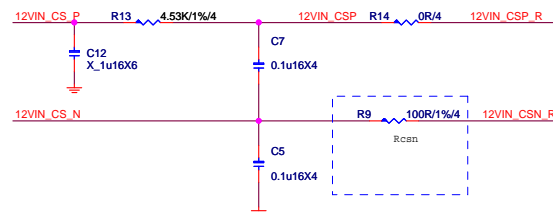
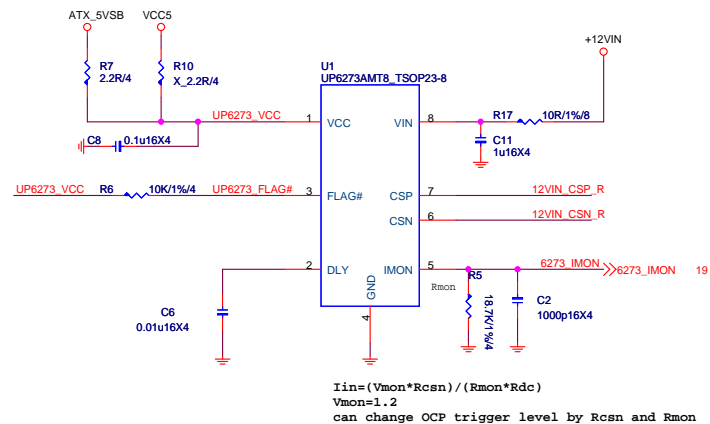
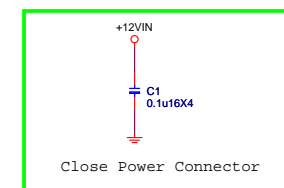


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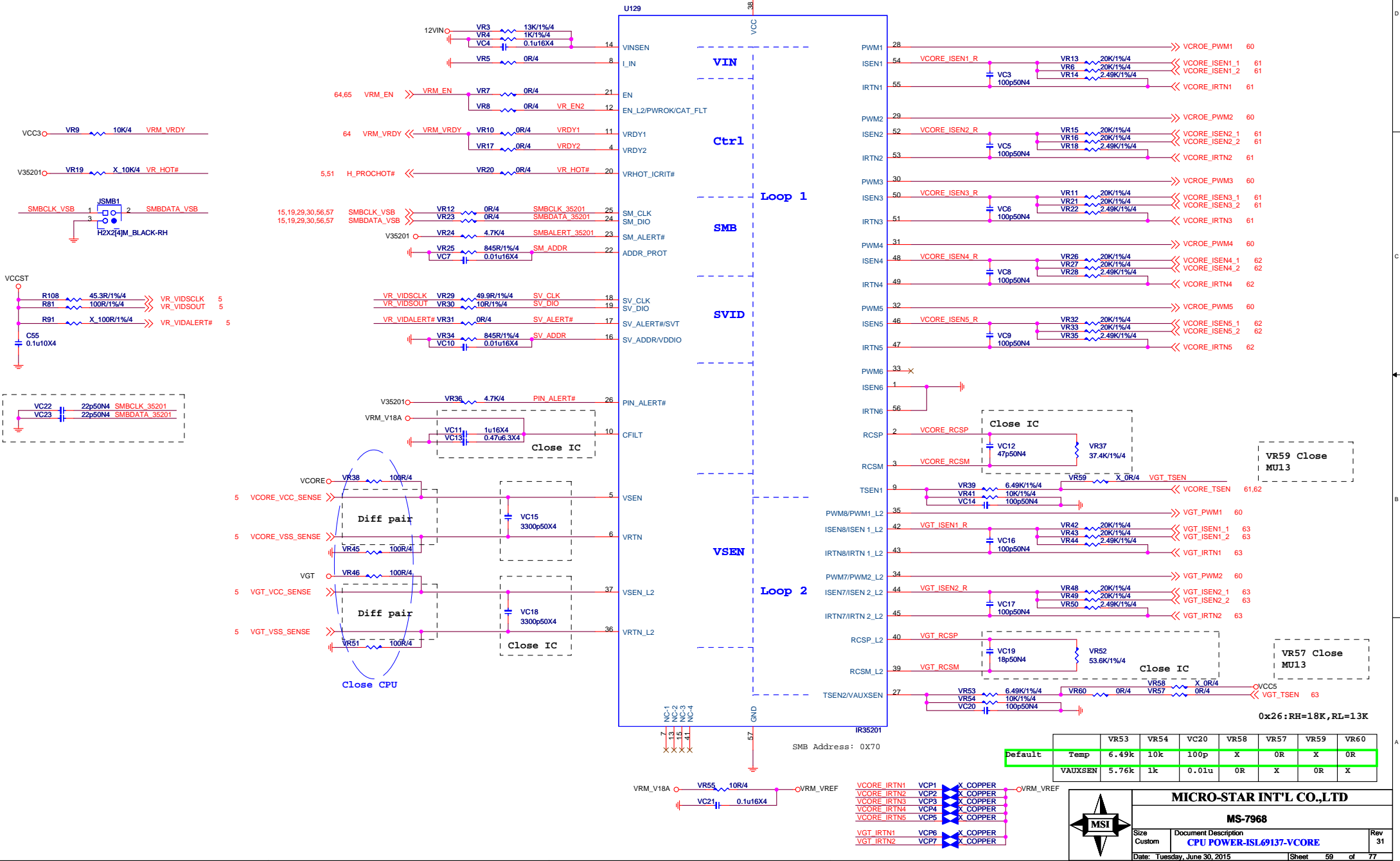
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POWER METER


[illegible]

Vcore: ICC Max 100A
LL: 2.1 mohm
OCP: 240A

VGt: ICC Max 51A
LL: 3.1 mohm
OCP: 88A



Default	Temp	VR53	VR54	VC20	VR58	VR57	VR59	VR60
		6.49k	10k	100p	X	0R	X	0R
		VAUXSEN	5.76k	1k	0.01u	0R	X	X



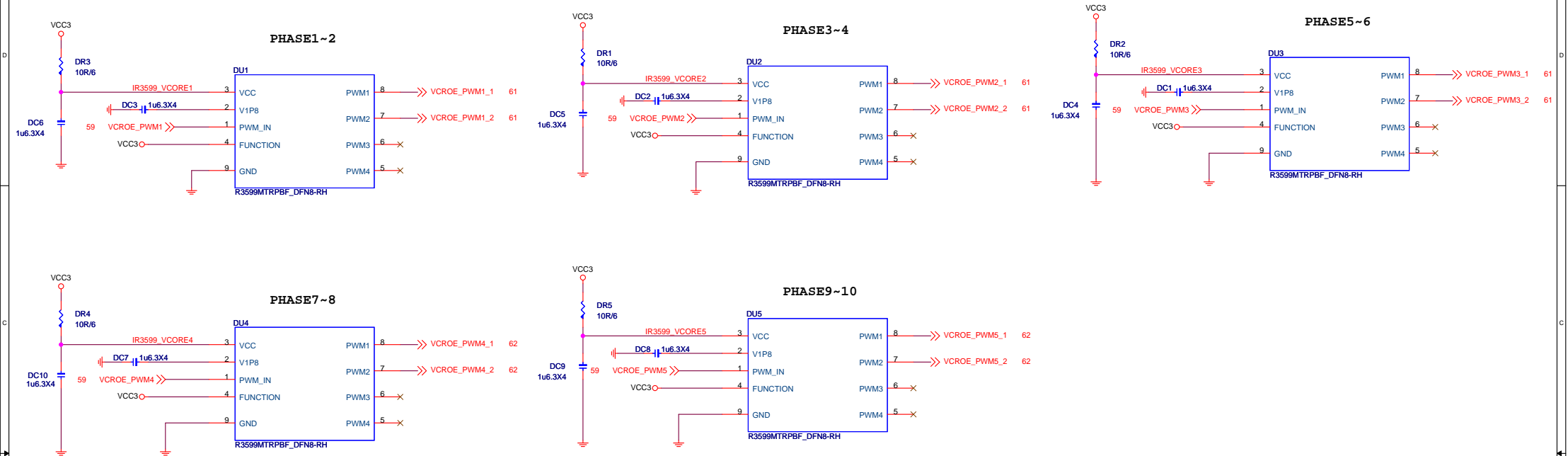
MICRO-STAR INT'L CO.,LTD

MS-7968

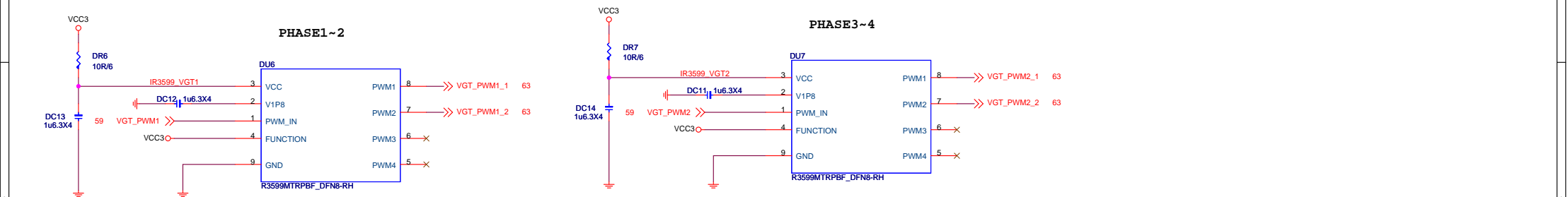
Size	Document Description	Rev
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VCORE Double



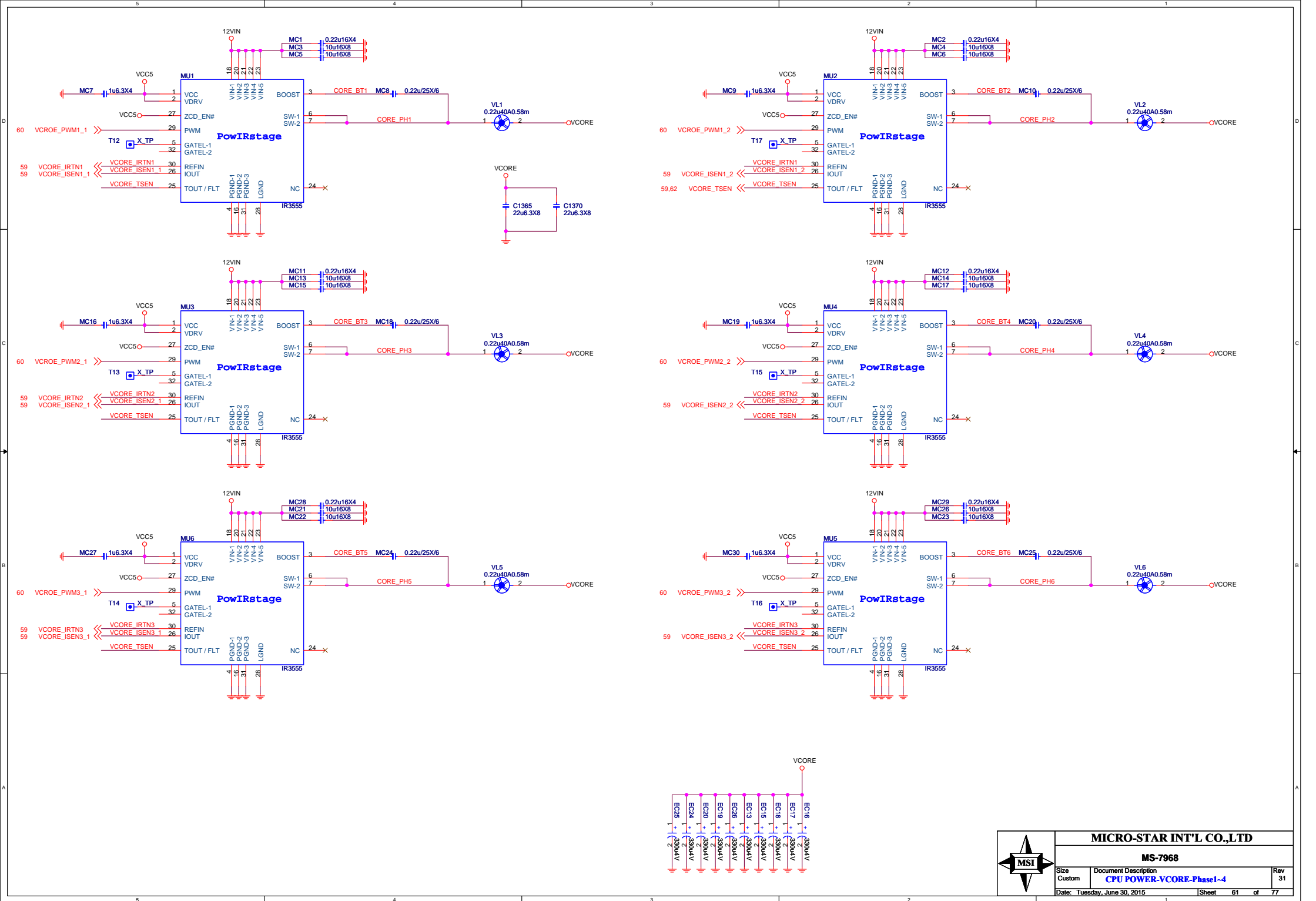
VGT Double

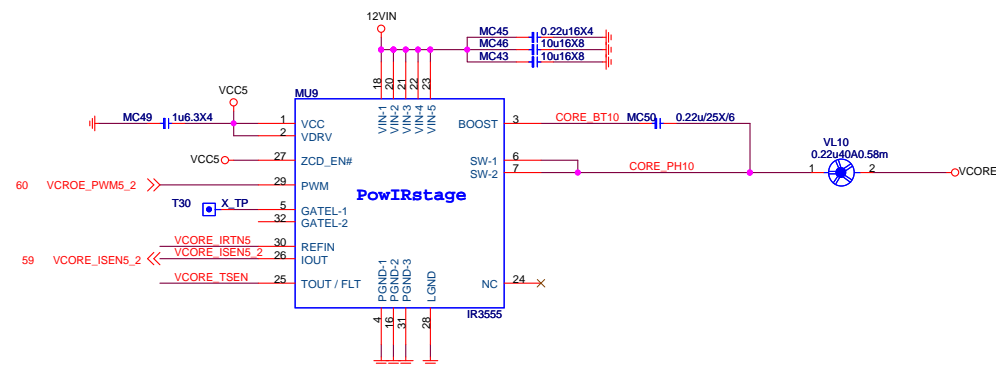
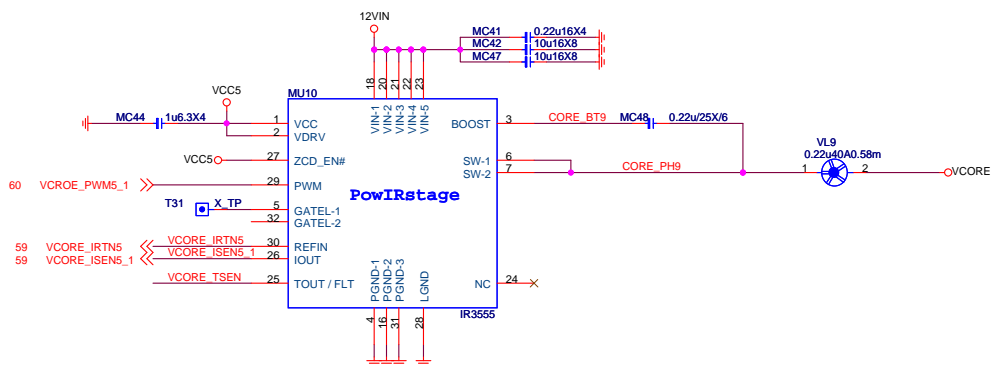
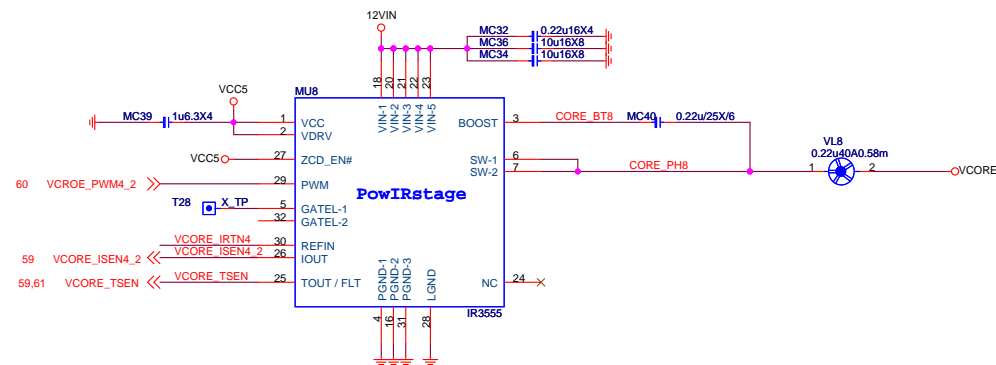
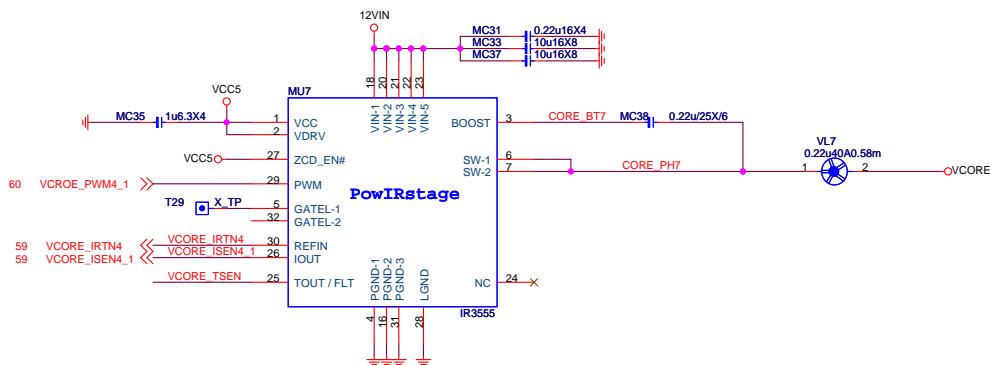


MICRO-STAR INT'L CO.,LTD

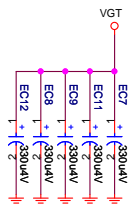
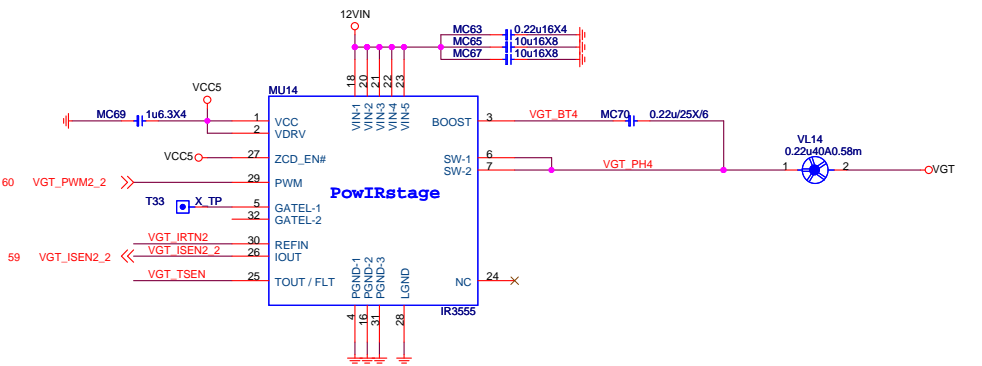
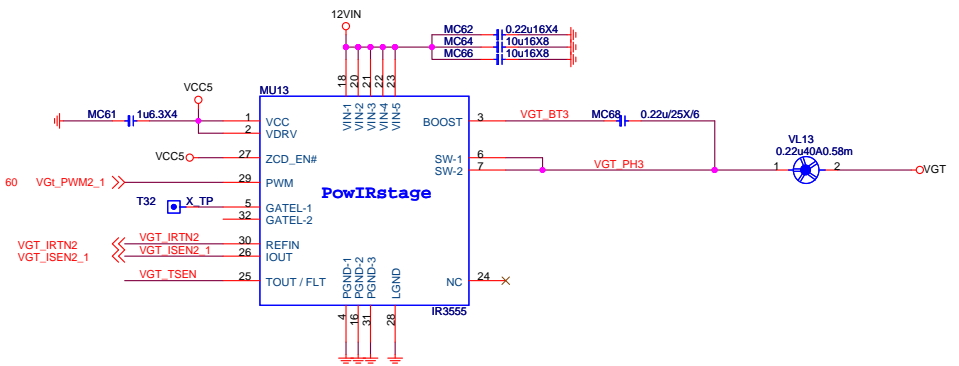
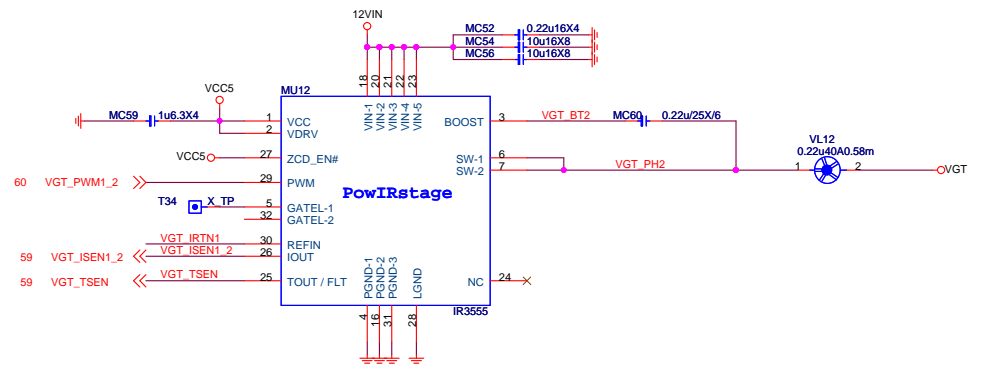
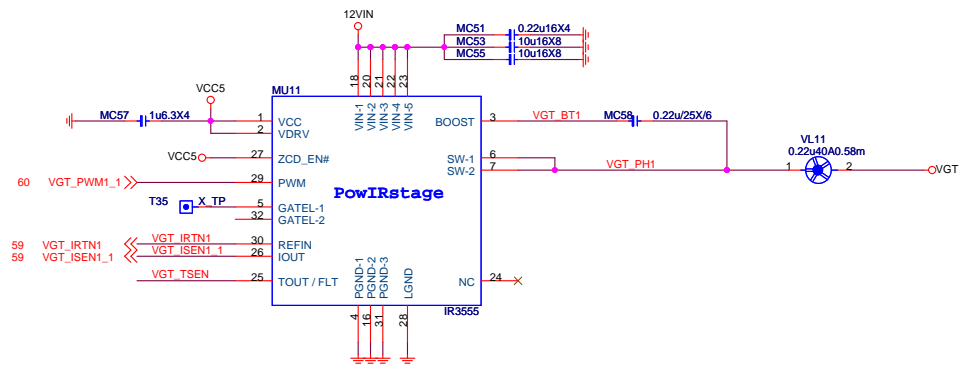
MS-7968

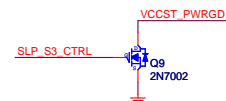
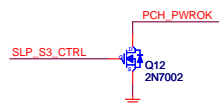
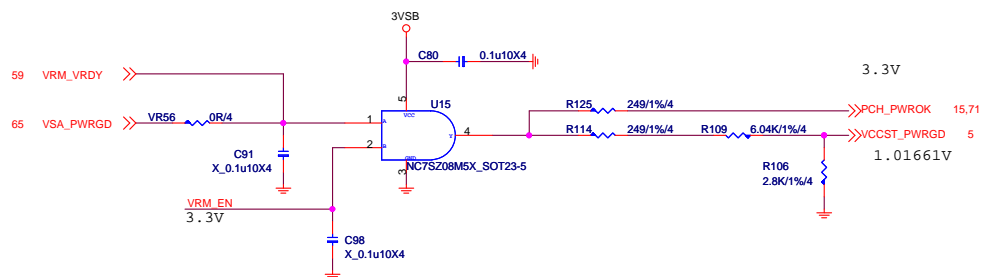
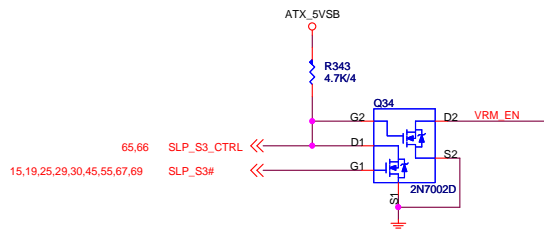
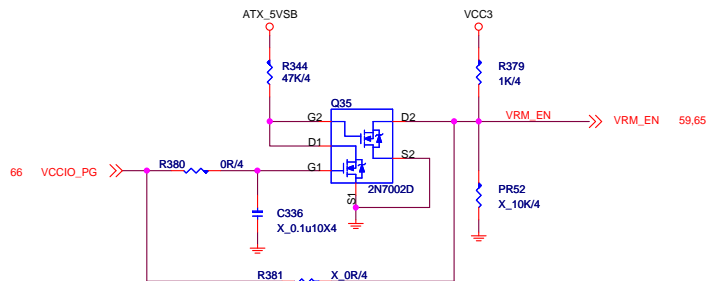
Size Custom	Document Description CPU POWER-ISL6617-VCORE	Rev 31
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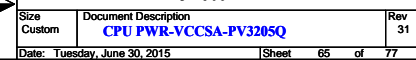


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OCP:XXA for 2Phase



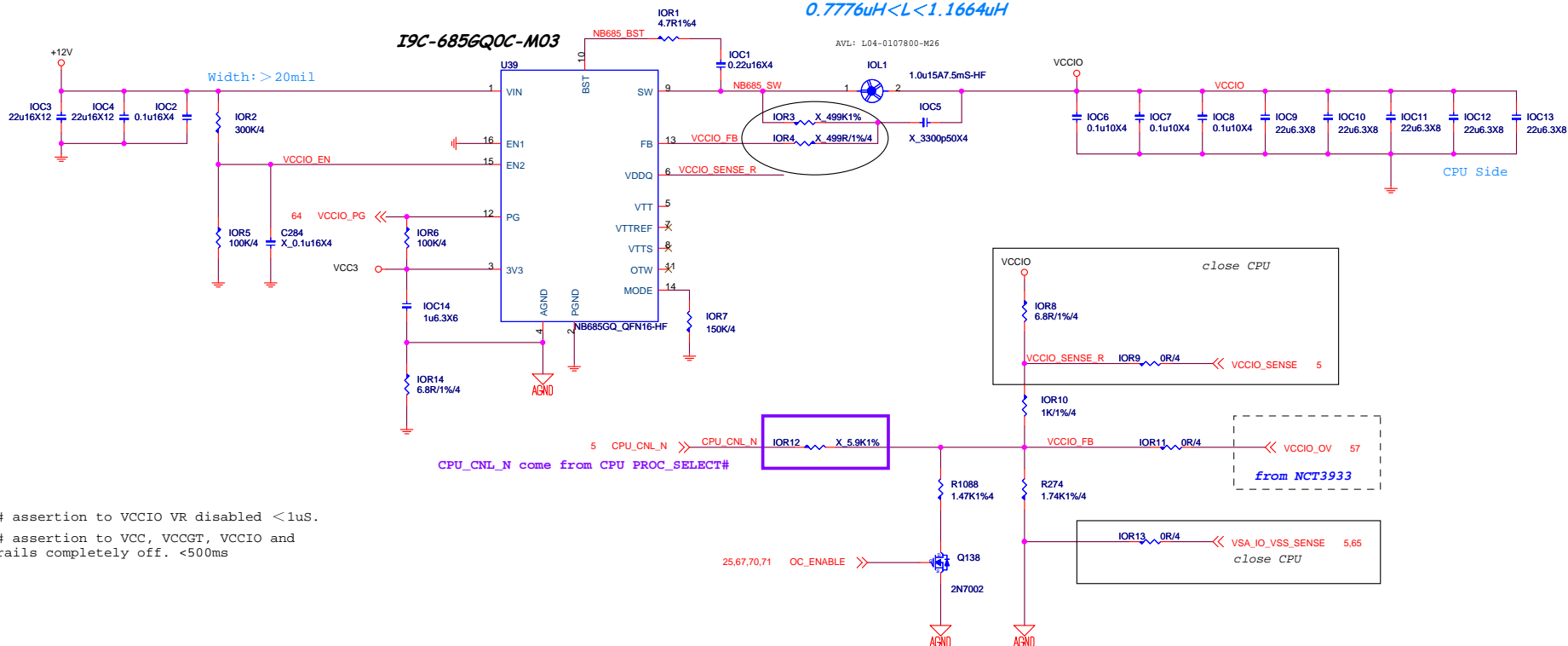
VCCIO

0.95V; 5.5A

support OV=>NB685

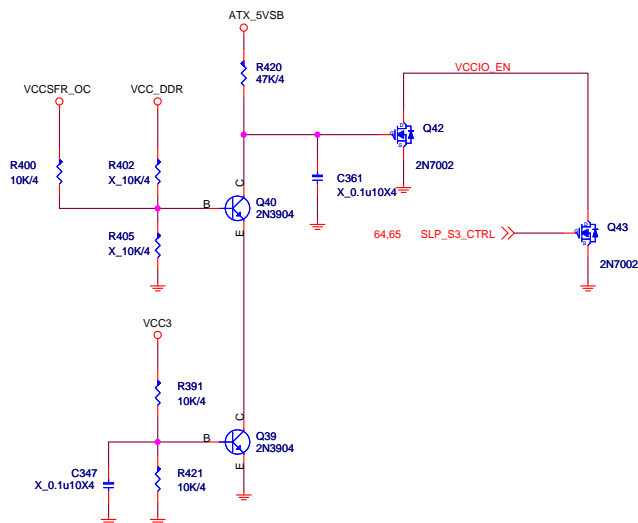
IMAX 10A
ILIMIT=10A~12A
IOC=ILIMIT+40%*IMAX/2=12A~14A.

0.7776uH<L<1.1664uH



SLP_S3# assertion to VCCIO VR disabled <1uS.

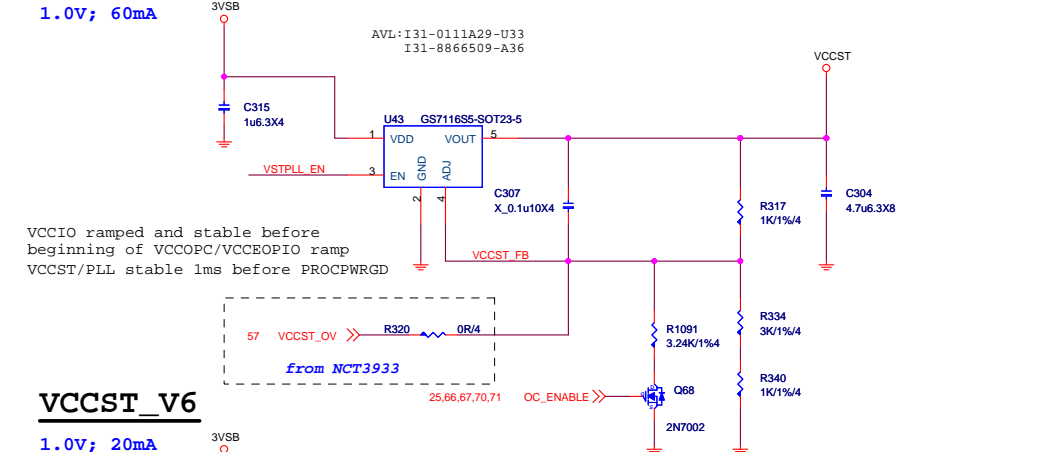
SLP_S3# assertion to VCC, VCCGT, VCCIO and VCCSA rails completely off. <500ms



only for OC & Gaming7/9/11

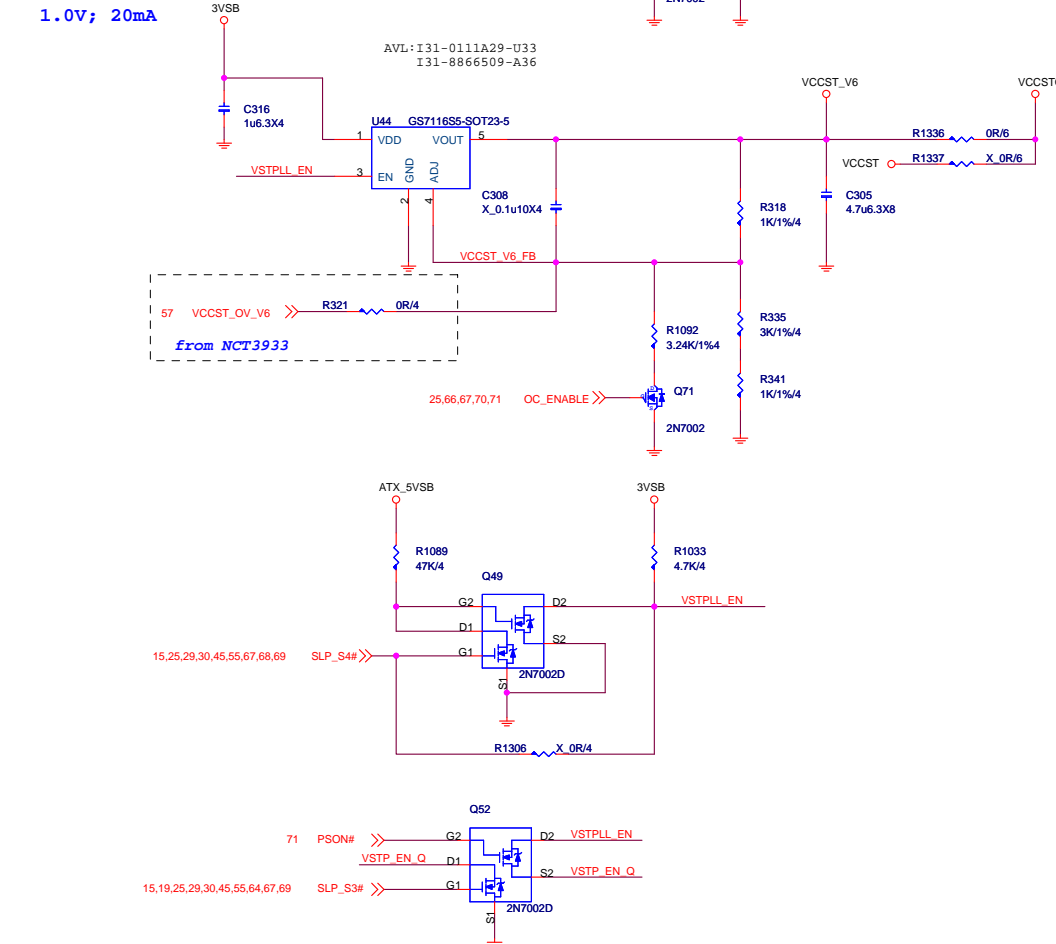
VCCST_V5

1.0V; 60mA



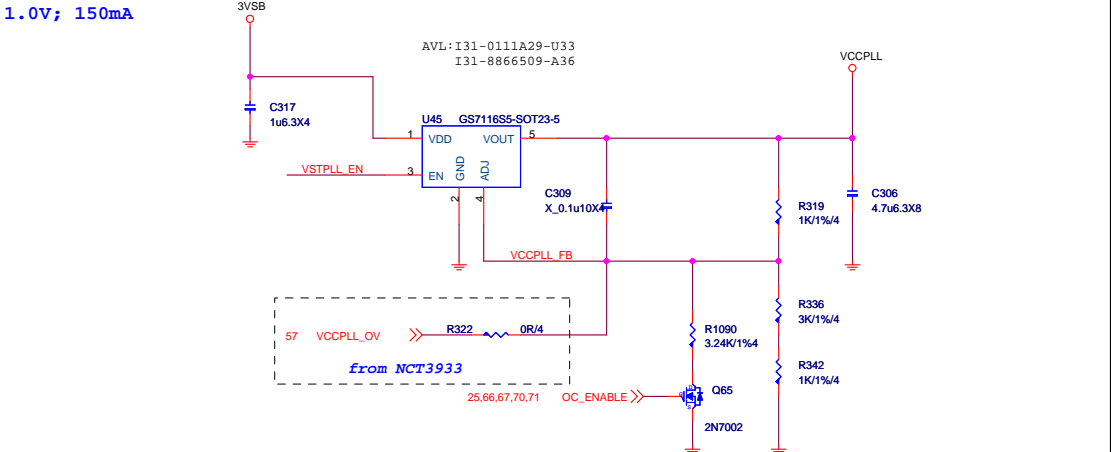
VCCST_V6

1.0V; 20mA



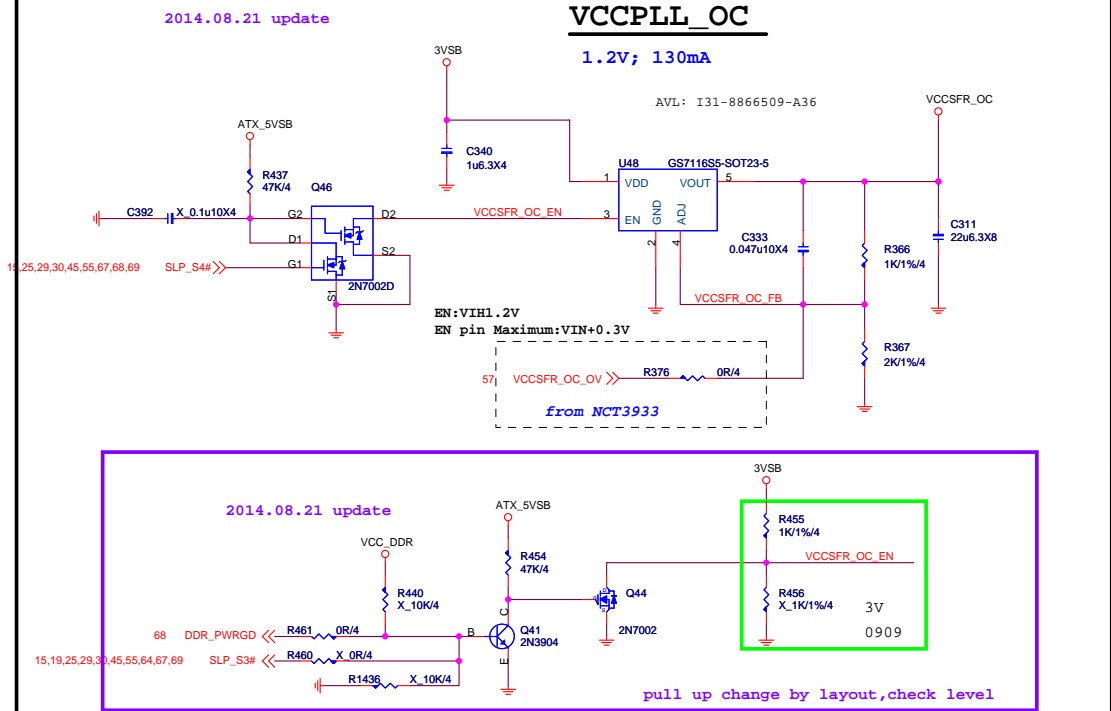
VCCPLL_V4

1.0V; 150mA



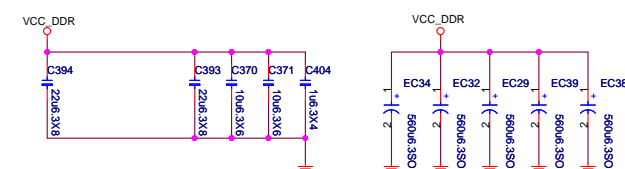
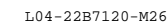
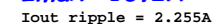
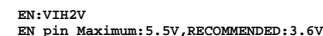
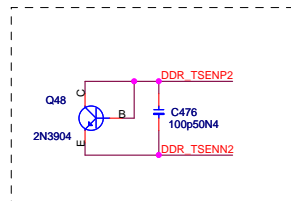
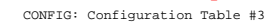
VCCPLL_OC

1.2V; 130mA



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Custom	CPU POWER-VCCST/PLL		31
Date:	Tuesday, June 30, 2015	Sheet	67 of 77

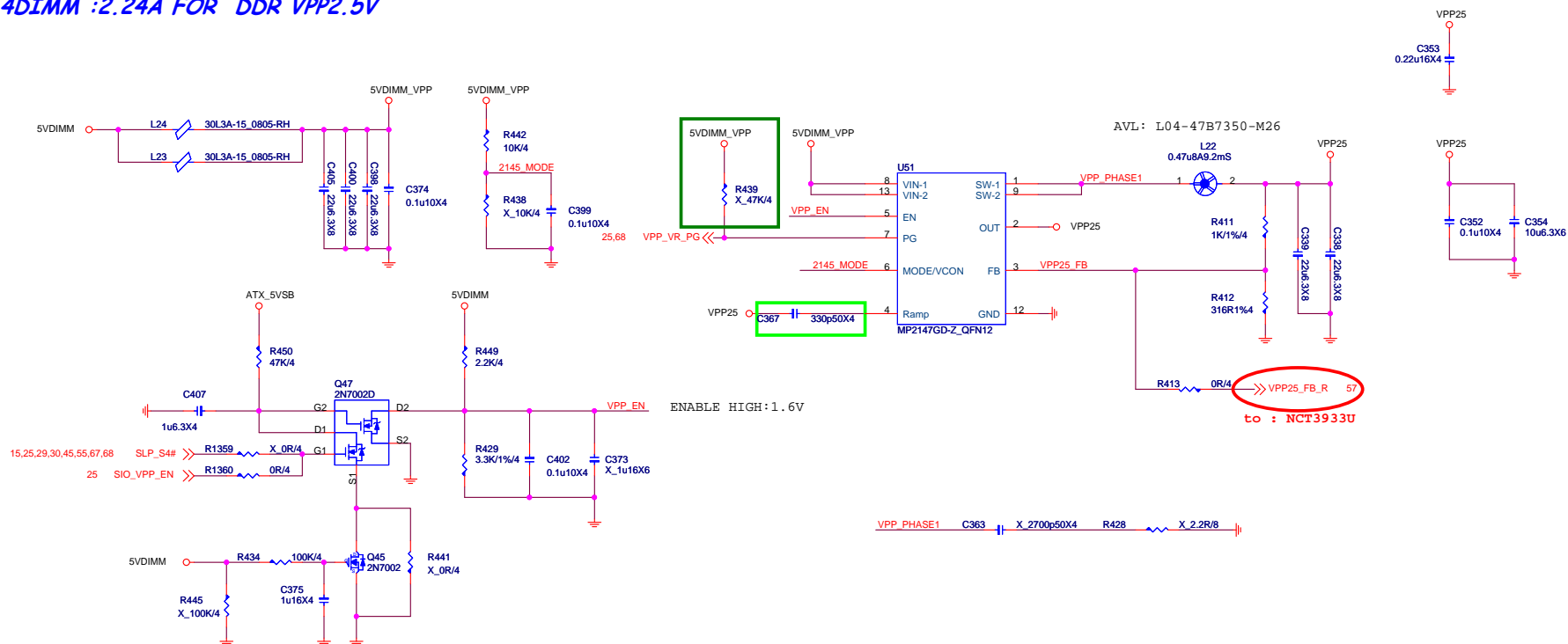
1.2A FOR DDR VTT



MS-7968

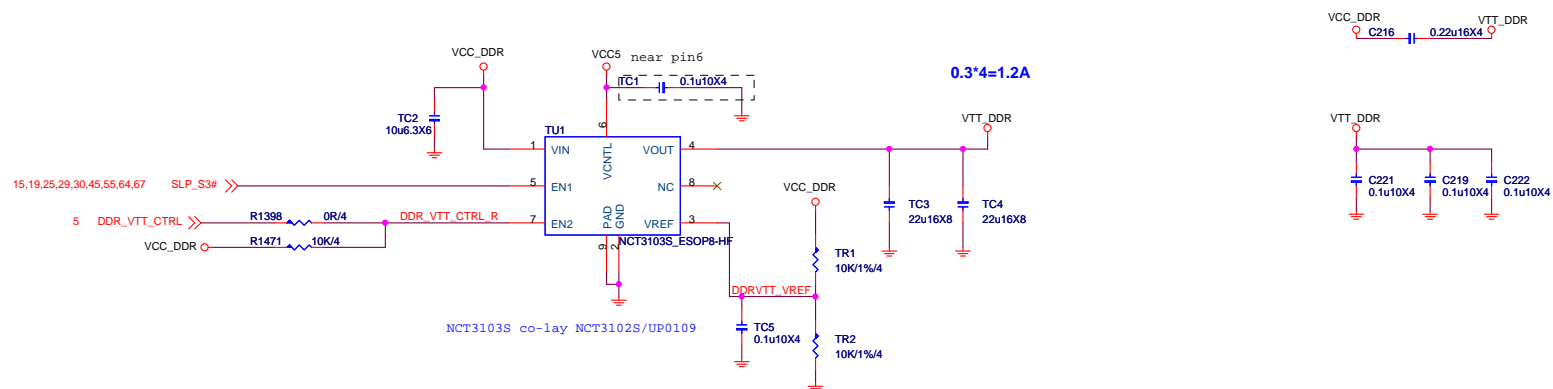
Size Custom	Document Description DDR PWR-PV3205Q	Rev 31
Date: Tuesdav, June 30, 2015		Sheet 68 of 77

4DIMM :2.24A FOR DDR VPP2.5V



DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .



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PCH_1VSB

1.0V; 10.664A

OCP = 16.21A

Rocset = 1.5 * I_{max} * R_{dson(LOW)} / I_{ocset}
 = 1.5 * 10.664 * 4.2mohm / 10uA
 = 6.71K

R_{dson(LOW)}

D03-4C05N03-005 : 3.4mohm
 D03-632BA0C-N03 : 3.3mohm
 D03-3056M00-U47 : 4.2mohm

$$I_{rms} = I_{out} * \sqrt{(V_{out}/V_{in}) * (1 - (V_{out}/V_{in}))}$$

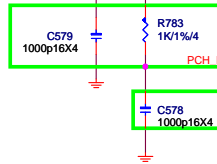
$$= 10.664 * 0.4$$

$$= 4.2656A < 5000mA$$

2014.12.25
 for up1540:
 C579 , R783 ->NC

2014.12.25
 For up1540:
 C578 is OCP set min:5K
 7.87K OCP = 15.74A
 For RT8125C stuff 1000P
 C11-1022032-W08

2014.08.21 update



MAX:10.664A

to sink/source over voltage IC.
 pin10 sink/source current capability can't over 1mA
 So max voltage can't over 1.8V.
 from NCT3933

$$V_{out} = V_{ref} * (1 + R_{821}/R_{822})$$

$$= 0.8 * (1 + 1K/3.92K)$$

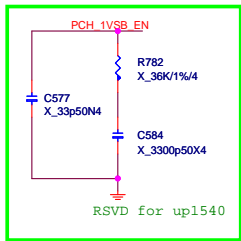
$$= 0.8 * 1.2551$$

$$= 1.004V$$

$$I_{min} = ((V_{in} - V_{out}) / (F_{sw} * k * I_{out_max})) * (V_{out}/V_{in})$$

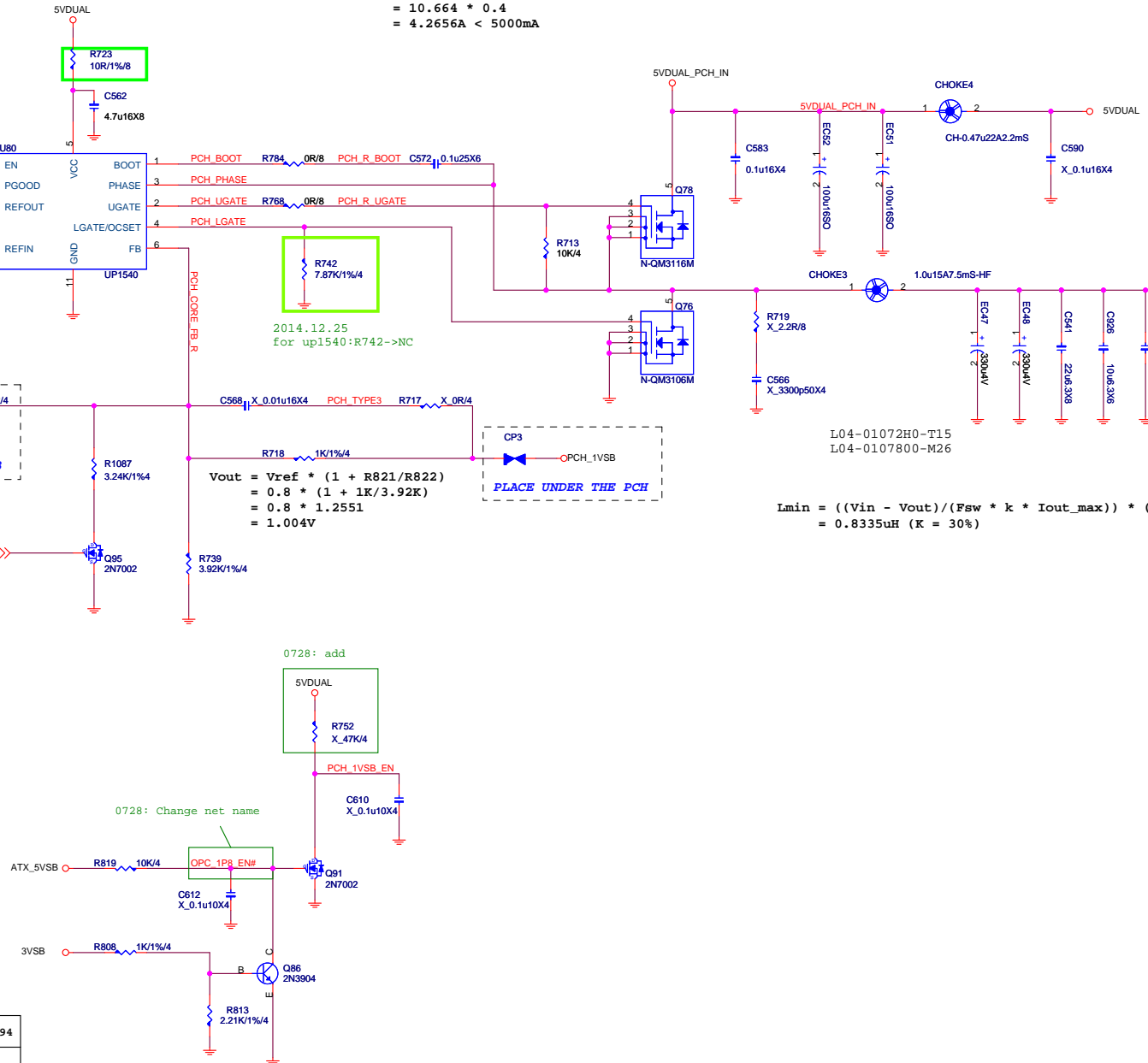
$$= 0.8335uH (K = 30\%)$$

29 HK_PCH_1VSB_OFF# R823 0R/4 PCH_1VSB_EN
 53 PCH_1VSB_EN# R824 0R/4



2014.12.25
 for up1540:stuff R782->36K,
 C577->330pF, C584->680pF

	C579	C578	R783	C577	R782	C584	R742	R1394
RT8125C I32-8125C0C-R11	1000P	1000P	1K	X	X	X	7.87K	X
UP1540Q I32-1540Q0C-U33	X	X	X	33p	36K	3300p	X	0R



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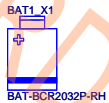
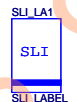
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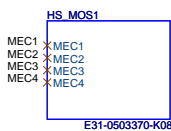
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PD1-0796831-E48,競華,10,寶安恩斯邁廠(MSIS)
PD1-0796831-G37,精成,23,寶安恩斯邁廠(MSIS)
PD1-0796831-G37,精成,72,寶安恩斯邁廠(MSIS)
PD1-0796831-G37,精成,23,寶安恩斯邁廠(MSIS)
PD1-0796831-G37,精成,2,寶安恩斯邁廠(MSIS)
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HEATSINK

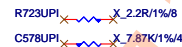


Cover

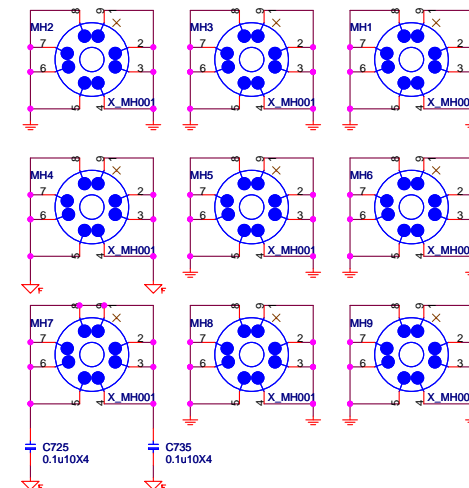


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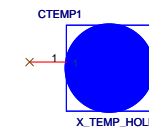
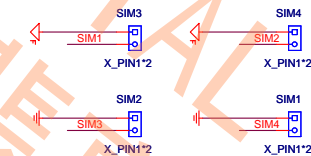
OPT PCH_1VSB



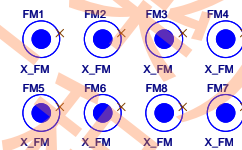
Mounting Holes



Simulation



Optical Fiducial Marks-120



- VCORE ○ □ VCORE1
- VGTT ○ □ VGTT1
- VCCSA ○ □ VCCSA1
- VCCIO ○ □ VCCIO1
- VCC_DDR ○ □ VCC_DDR1
- VTT_DDR ○ □ VTT_DDR1
- PCH_1VSB ○ □ PCH_1VSB1
- 5VDUAL ○ □ 5VDUAL1
- 5VDIMM ○ □ 5VDIMM1
- 3VSB ○ □ 3VSB1
- VBAT ○ □ VBAT1
- VPP25 ○ □ VPP1



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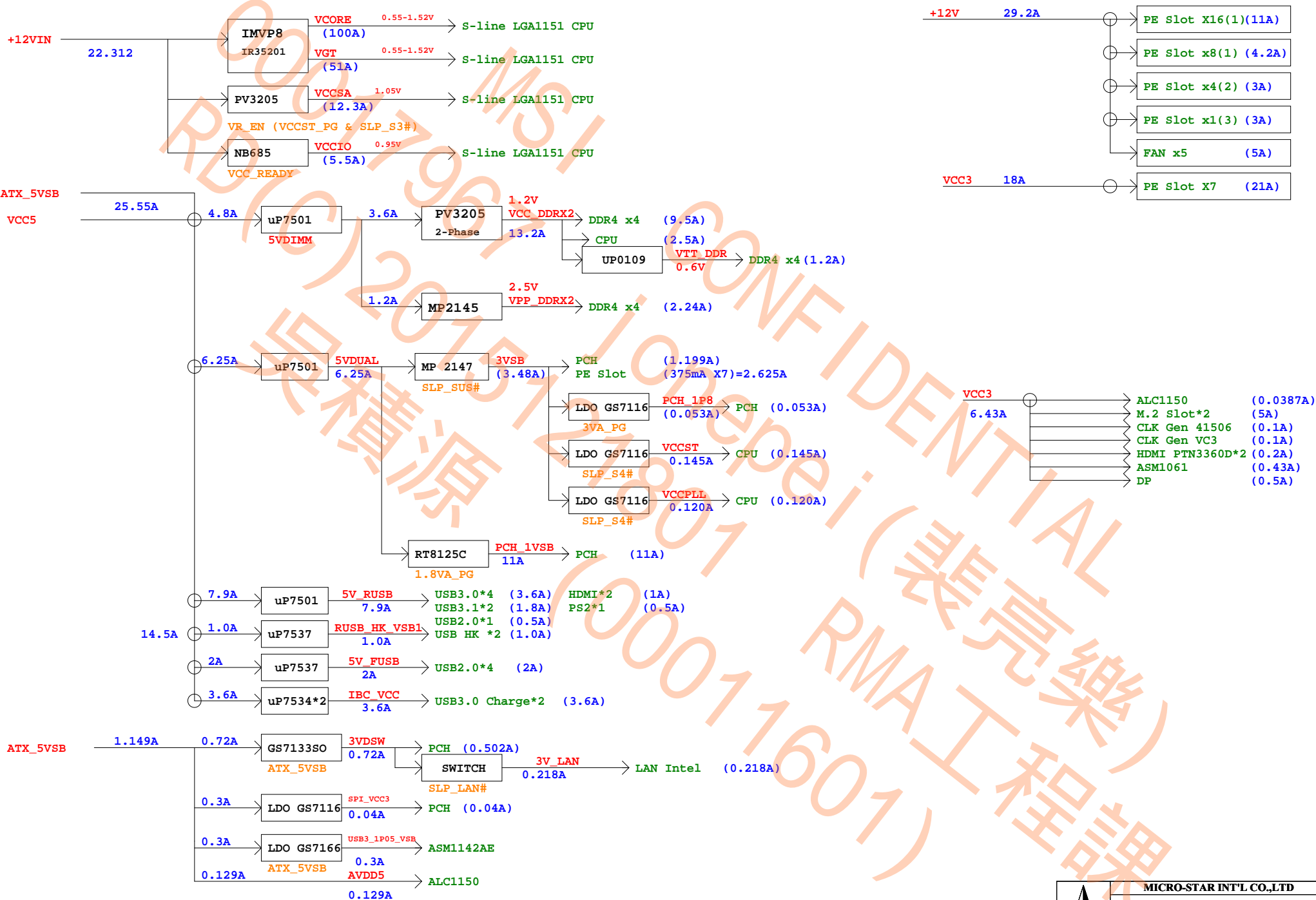
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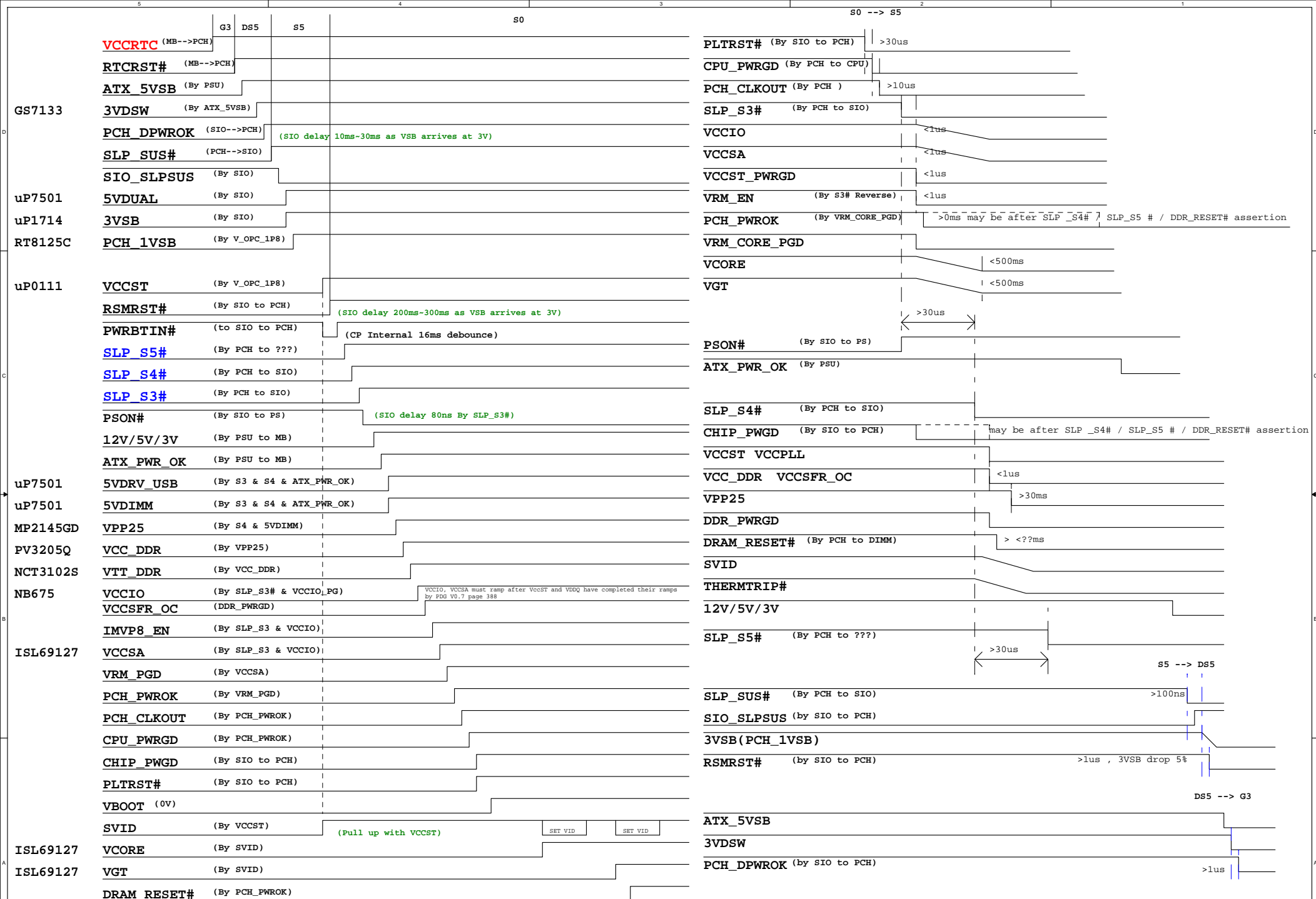
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Power Delivery

CPU TYPE
(4+2)





0A to 0B

Update CPU and PCH LIB

Page 4 Add R1410,TP97,TP98 For internal test
Page 5 Add CFG9,CFG14,CFG15 CTRL circuit
Page 6 Stuff C874
Page10 Change VCC_DDR to DIP Cap,Add C941,C942,C943,C944,C945,C946
Page13 Remove R1187,R1191,R1190,R1195,R1182,R1181,R1183,R1186,R1179,R1180
R1196,R1204,R1203,R1209,R1206,R1212,R618,R614,R634,R619,R1218,R1213

Page14 Remove R663,R1223,R664,R1210,R629
Add R1353,R1355,R1357,R1352,R1354,R1356,R1412,R1423,R1424
Page15 Change Value R1275 150K,R792,R793 20K
Page16 Remove R786 Group_A Co-lay PCH_1P8
Page19 Add FS Ctrl circuit
modify SMBUS co-lay circuit

Page25 Change PWRBTIN pull up Resistor to SIO side
add C1338 for ESD
add R1338,R1339 for SLPSUS leakage
add R825,C615 for auto clean CMOS
R577 un-stuff
CHARGE_CB change to GP16
For 6793 RevA
Add DDR4 Sequence circuit
LED_VCC to GP10
LED_VSB to GP11
remove ESPI function and 1P8 Power

Page27 Change FAN Module to Type I
Page28 Change FAN Module to Type H

Page29 Modify Hot_key1 circuit
Page30 Add R1344,R1345,R1346,R843,LED14,D30,D31
un-stuff R835,co-lay common choke for EMI

Page32 Remove X'tal
Add U99 for VC3 soft-start

page42 modify IFDET circuit.
page43 simplify M2_1,SATA,SE1 switch circuit
page44 simplify M2_2,SATA, switch circuit
Page45 co-lay common choke for EMI
Page46 co-lay common choke for EMI
Page47 co-lay common choke for EMI
Page48 co-lay common choke for EMI
Page49 co-lay common choke for EMI
Page50 stuff R1140
page51 change J1 to housing type
Add R1397
page52 Add Q169,R1421
Remove R1014
page54 R766 change to 20.1k
page56 Add VCO_EN for CLK Gen
page57 Add PCH_CLK5_1P0 for PCH ICC power OV
page58 Change value R9 57.6,R13 4.53K
Page59 Change Current Sense to DCR Mode
R64 4.02K,R85 1K
Add R1422
Page66 Change pwm to PV3205Q
Page71 Remove U85 PCH_1P8
Page72 Add J2 for Dual PSU

0B to 30

Page 5 add R1425 Pull high to VCCST
Page 6 add C256 change to VCCSA
Page 14 add R618,R619 for XMP LED
remove R595,R594
Cheange net name PCH_X4_SEL2 to PE4_SEL
Page 21 Add C1366 for SA Reset Issue
Add C1367,C1368 for SA Reset Issue
Page 23 Add R1430,R1431,R1432,D35,D36,D37
for PCI_E2,PCI_E4,PCH_E6 PRSNT Ctrl logic
Change R514 to 100R for SA Reset Issue
Page 24 Remove Q123,Q122 and Add Q159,Q160,Q161
for PCH X4 and X1 mode Ctrl logic
Page 25 Remove R588,C528,RT1
Stuff R589
Page 26 Remove Post3,Post4
Page 27 add FC41,FC42,stuff FQ1,FQ2
Page 28 FC43,FC44,FC45
Page 33 Change RU10 to 5.1K
Page 34 Remove R891,LED12,Q109
Page 43 Remove R591,LED9,Q68
Page 44 Remove R966,LED13,Q118
Page 45 F1 change footprint to USMD100
Page 46 F6 change footprint to USMD100
Page 47 F7,F8 change footprint to 0805
Page 48 F4 change footprint to 0805
Page 49 F2,F3 change footprint to 0805
Page 51 Add OC1 HW,SW LED ctrl circuit
Page 52 Add Q170 fixed Dual BIOS LED issue
Page 58 Change R5 to 100R,R9 to 18.7K
unstuff Q138,Q139,R1057,R1056

Page 59~63 Change PWM to IR
Page 67 Add R440,R1436 for PV3205 PWRGD issue
Page 69 Change DDR_VTT to NCT3102S
Page 70 unstuff R713
Page 71 add Unfreeze CTRL circuit

30 to 31

Page 5 Remove R1400,R1402,R105
Page 6 Change VGT MLCC to 22uF
Page 14 Change R619 Pull Down to GND
Change OC1 GPIO to PCH1.AM44
Remove Some OR and TP
Page 15 R1235,R1233 stuff,add R1449
Page 16 Add R1292 by MOW23
Page 19 Add IMON and Cut power circuit,
Add D36 for Seq
Page 27 unstuff FC41,FC42
Page 28 unstuff FC43,FC44,FC45
Page 29 Change U17 power to 501_5VSB
Page 30 Change U83 power to 504_5VSB
Page 31 unstuff R994,R995 change to 4.7k
Page 52 Add D33,unstuff R912
Page 53 Add R490,Q258,R1466,C1377
Page 57 Add R1098,R1467
Page 59 VR37 to 37.4K
VR52 to 53.6K
VR25 to 845R
Page 63 Remove EC58~61
Page 66 Add Power on change voltage circuit
Page 67 Add Power on change voltage circuit
Page 69 Add R1471
Page 70 Add Power on change voltage circuit



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